I-fuse™: A Disruptive OTP Technology

Jeffrey Lin/Shine Chung
May 5, 2019

Attopsemi Technology

1A2-A1 No. 1 Li-Hsin 1st Rd, Hsinchu, Taiwan 300-78

☎886+(3)666-3150x211, 886+920-566-218

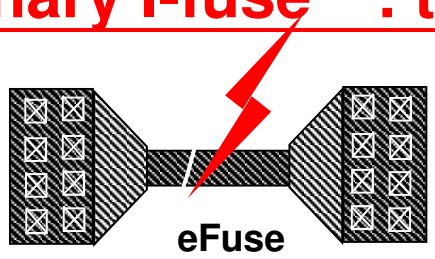
About Attopsemi Technology

- **Founded in June 2010**
  - By a team of semiconductor veterans and experts
- **Located at Si-Soft Research Center of Hsinchu Science Park, Taiwan**
- **Biz: OTP (One-Time Programmable) IP development and licensing**
  - Foundry independent OTP; no additional masks or process steps
  - Program not by NVM ways: break fuse, rupture oxide or trap charges
  - But by "true electromigration: accelerating wear-out of logic devices"
    - 100x reliability, 1/100 cell size, and 1/10 program current of eFuse
    - Pass HTS @300°C for 4,290 hr; defect rate <0.01ppm; fully testable
  - Universal and proven OTP from 0.7um to 22nm and 7nm and beyond
- **Patent portfolio: >65 filed in US and 11 in Taiwan/China**
- **Engaged >15 foundries and >50 customers worldwide**

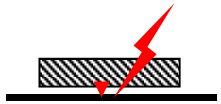
Different OTP Technologies

- **Store data Permanently but Program Once**
  - NVM device
- **Other OTP: NVM mechanisms**
  - Break fuse, Rupture oxide, or trap charges in floating gates
- **Other OTP: NVM Problems**
  - Large size, HV PGM, charge pumps, hard to use, low reliability
- **Revolutionary I-fuse™: true logic device OTP to win**

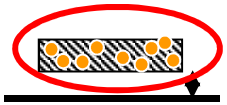
I-fuse™



eFuse



Oxide rupture

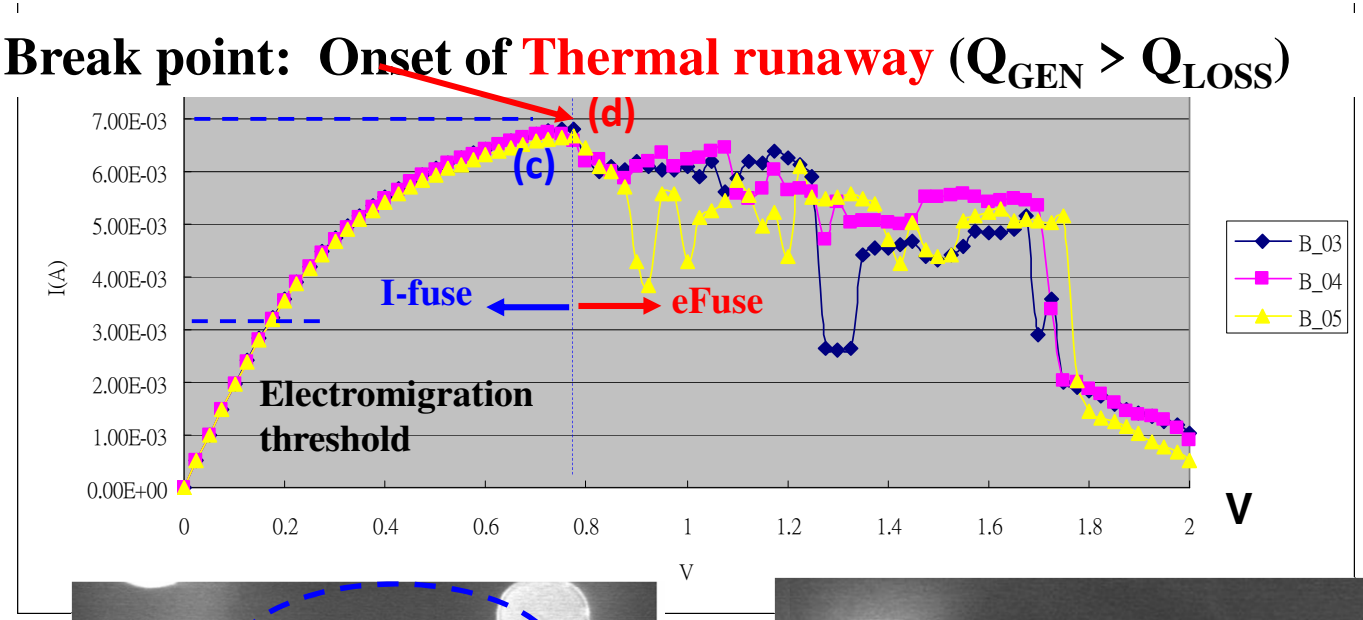


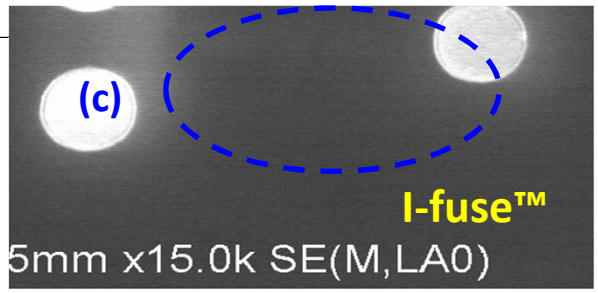
Floating-gate

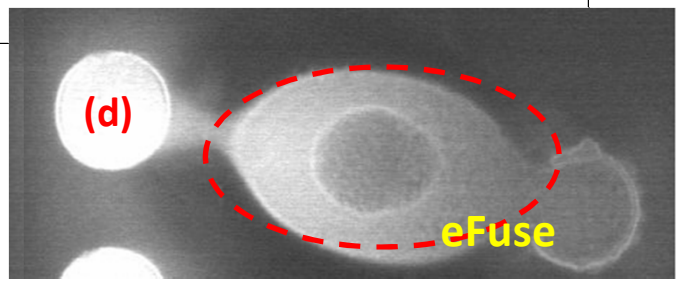
Non-break fuse	Break fuse	Rupture oxide	Trap charges
Deterministic	Explosive	Explosive	Statistical
≦0.6um	≦0.18um	≦ 0.18um, ≧14nm	≧0.35um, ≦ 0.6um
<0.01ppm defect	29ppm defect	10ppm defect	100ppm defect
No problem	Grow back	Self-healed	data retention

I-Fuse™ vs. eFuse Programming

- I-fuse™: non-explosive fuse; Guaranteed reliable by physics
- eFuse: explosive fuse => create debris => grow back





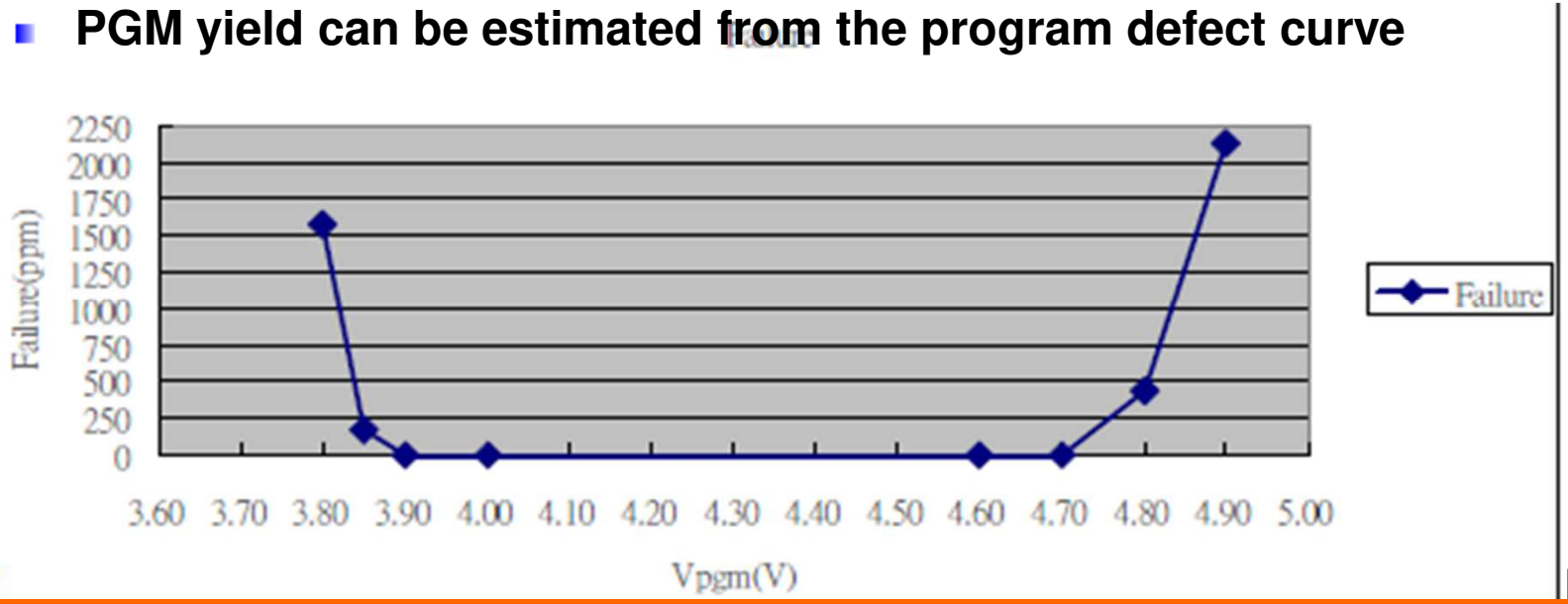


(UD50SP)

Power devices should not operate in thermal runaway. So programming a fuse should not.

I-Fuse™: Programming

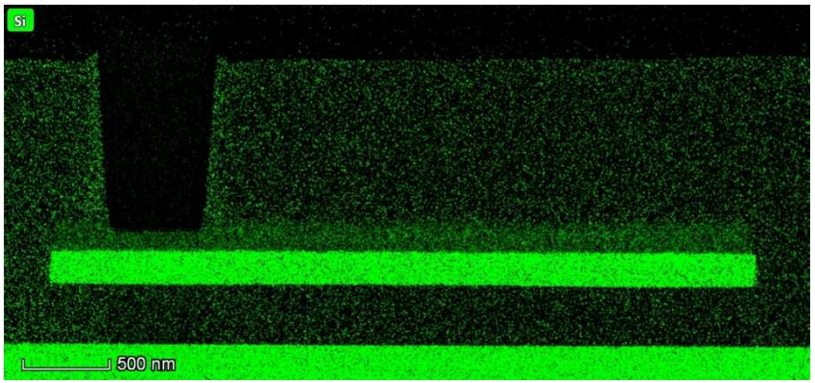
- **eFuse:** apply voltage to spec; generate a high current to blow eFuses
- **I-fuse™: has a natural program window**
  - Program window can be adjust by cell size, I-fuse™ structure, etc.
- **I-fuse™ program window characterization**
  - Start with a very low voltage to PGM I-fuse™
  - Increment PGM voltage until all bits can be PGM'd—Low Bound (LB)
  - Increment PGM after LB until read failure--- exceeding High Bound (HB)
  - Set the typical PGM voltage as average of LB and HB
  - PGM yield can be estimated from the program defect curve



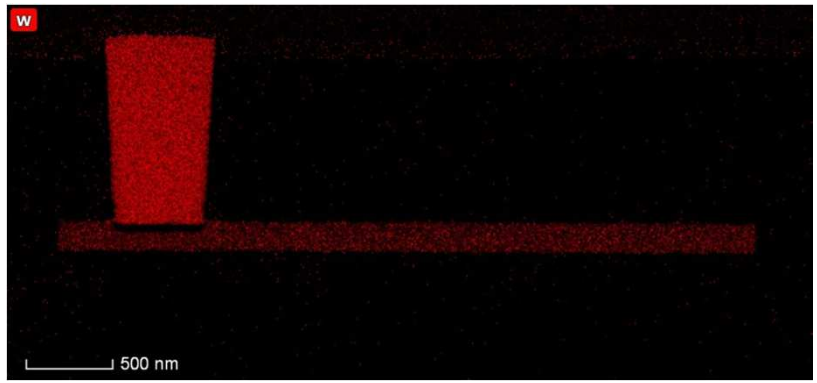
TEM/EDX of I-fuse™ on WSi2 (1/2)

Un-Programmed

- Before program, W is uniformly distributed



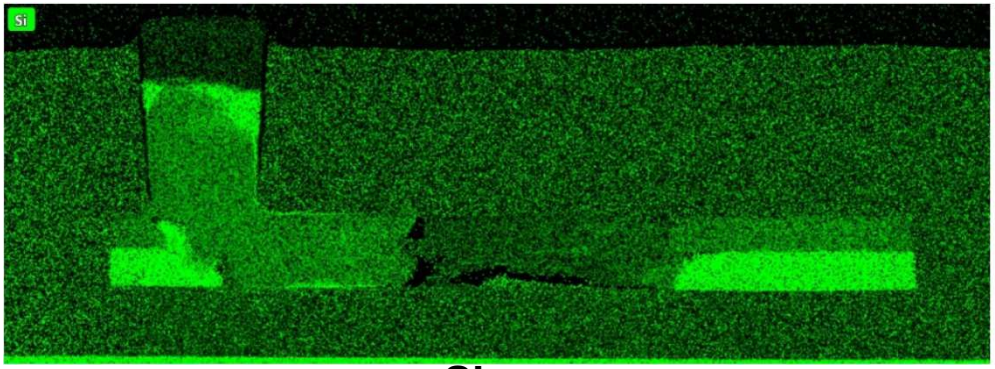
Si



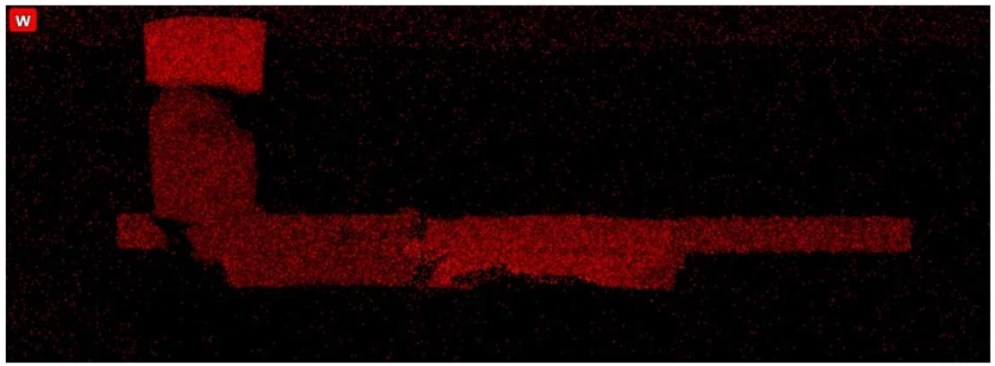
W

PGM below LB

- Insufficient PGM: some W got insufficiently migrated



Si

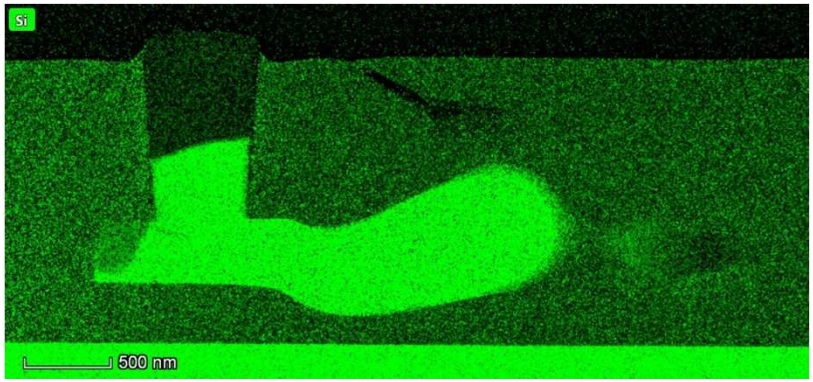


W

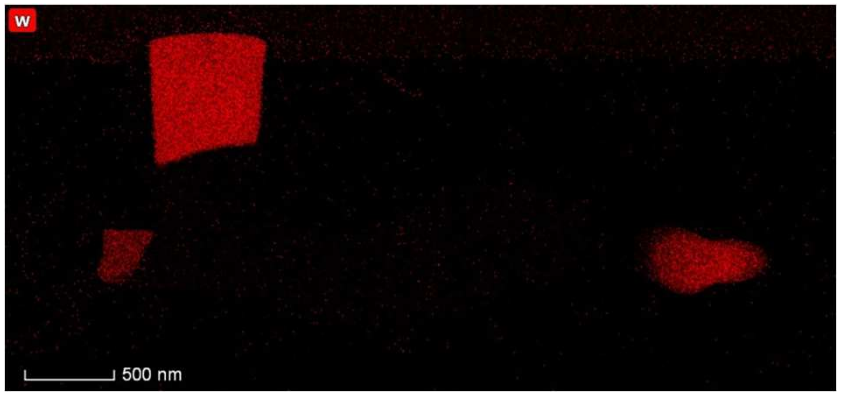
TEM/EDX of I-fuse™ on WSi2 (2/2)

I-fuse™ PGM

- After program, W migrated to anode; Si intact



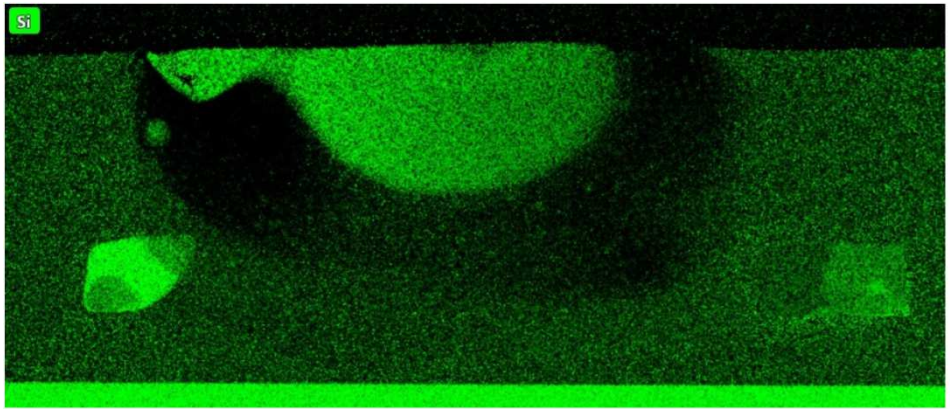
Si



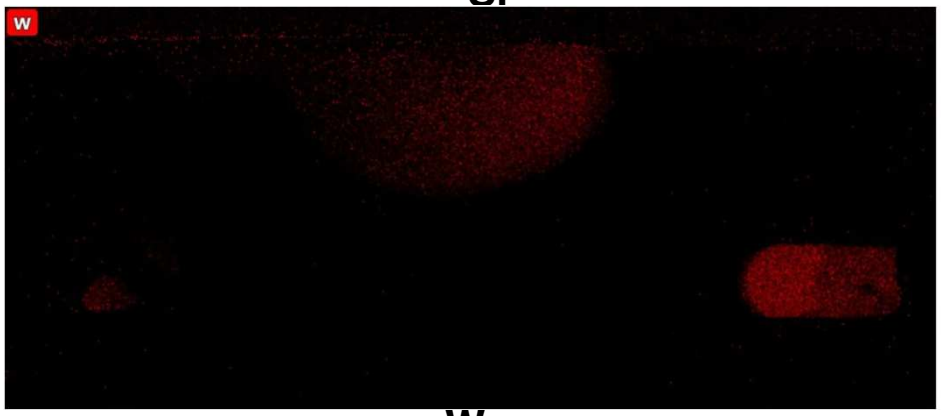
W

PGM over HB

- Si got severely damaged, W scattered around



Si



W

Reliability of a Fuse After Burn-in

- **I-fuse™ works in the reliable typical/under programming regions**
  - **Under-programmed poly: R↑ after burn-in (O.K.)--- I-fuse™**
  - **Typical programmed poly: R unchanged (O.K.)**
  - **Over-programmed poly: R ↓ after burn-in (Bad)**
- **Reasons:**
  - **Under-program: Burn-in increases fuse resistance => read margin↑**
  - **Over-program: Debris after explosion may bridge to create shorts**

Typical Programming

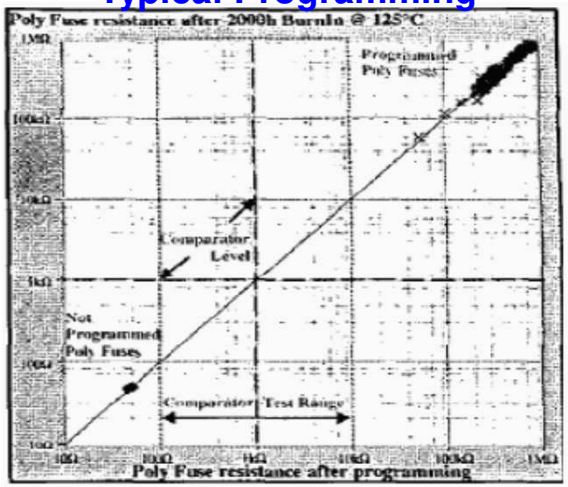


FIGURE 7. LIFETIME DRIFT OF A TYPICAL PROGRAMME POLY FUSE

Under Programming

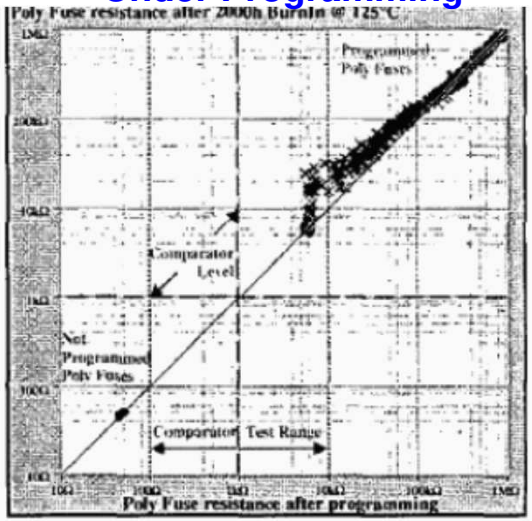


FIGURE 8. LIFETIME DRIFT OF A POLY FUSE PROGRAMMED AT LOWER PROGRAMMING CURRENT

Over Programming

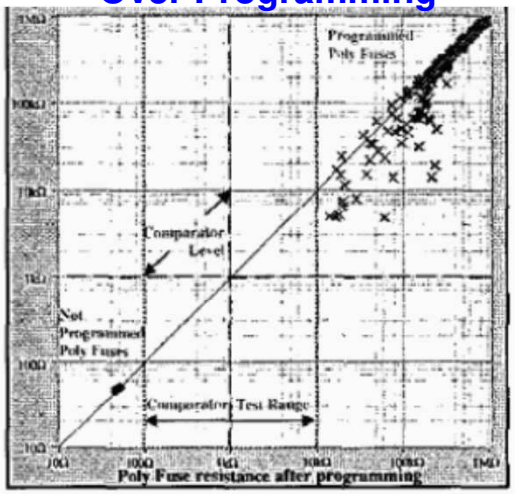


FIGURE 9. LIFETIME DRIFT OF A POLY FUSE PROGRAMMI AT HIGHER PROGRAMMING CURRENT

0.35um Polysilicon TiSi2 eFuse Reliability

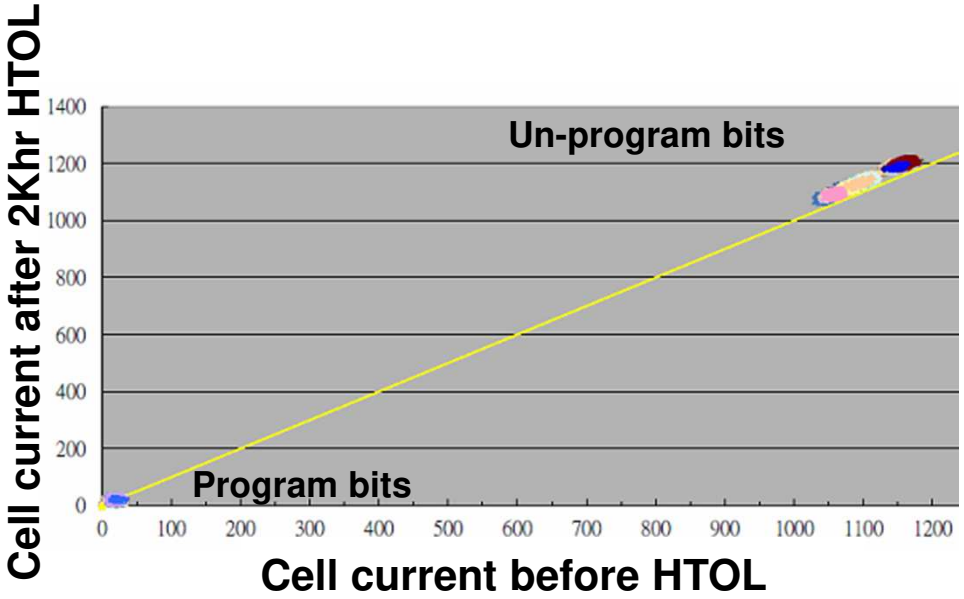
- *Authors show HTOL results for eFuse that is programmed at nominal, low, and high programming currents. Some drift is noticed at other than optimal programmed level, indicating initial programming criterion is key for an optimized fuse geometry.*

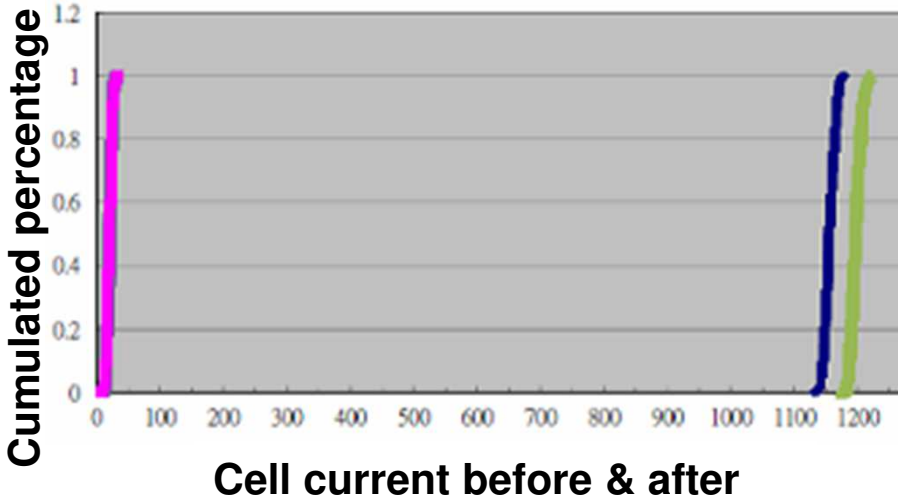
"Lifetime Study for a Poly Fuse in a 0.35µm Polycide CMOS Process", J. fellnar, P. Boesmueller, H. Reiter, IEEE IRPS 2005 Proceedings pg 446-449,

I-Fuse™ Passed 150°C HTOL, 2Khr

- **I-fuse™ passed HTOL 150°C, 2,000hr to AEC-Q100 Grade 0 qual**
  - **Cell current distributions for pre-/post PGM cells are narrow**
  - **Separation between pre-/post PGM cells are far apart**

- **Cell current variation after stress vs. before stress (32Kb)**
  - **Pre-PGM cell currents decreased --- additional annealing for fuse**
  - **Post-PGM cell currents virtually didn't changed**





eFuse Resistance after HTS

- **eFuse has more than 10x resistance change after bake**
  - **For Xlinx's paper at 65nm and IBM's paper at 90nm**

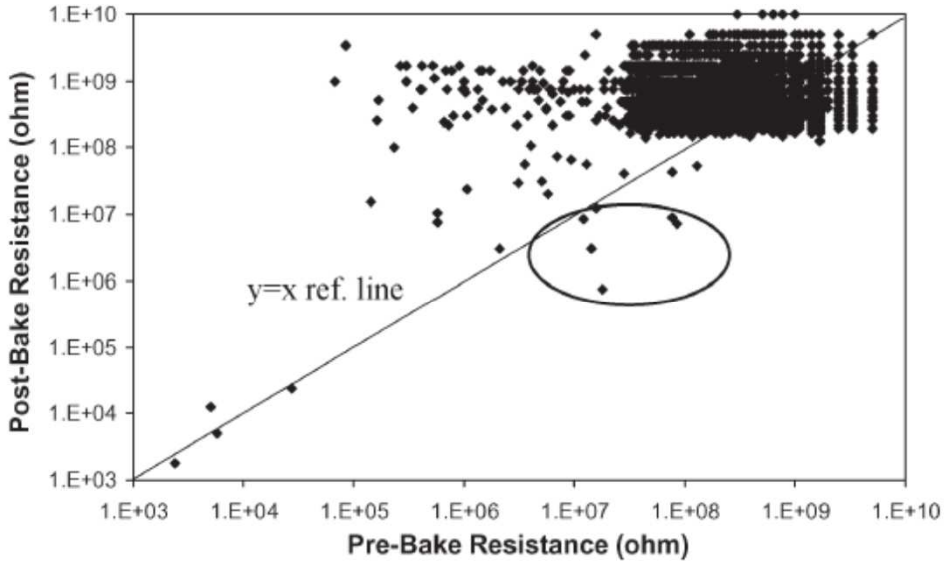


Fig. 7. Prebake and postbake resistance of well-programmed fuses. Bake condition: 1000 h at 250 °C. (circled) A few bits show resistance reduction after bake; however, their resistance is still well above the sensing circuit trip point.

NiSi Polysilicon Fuse Reliability in 65-nm Logic CMOS Technology

IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, VOL. 7, NO. 2, JUNE 2007

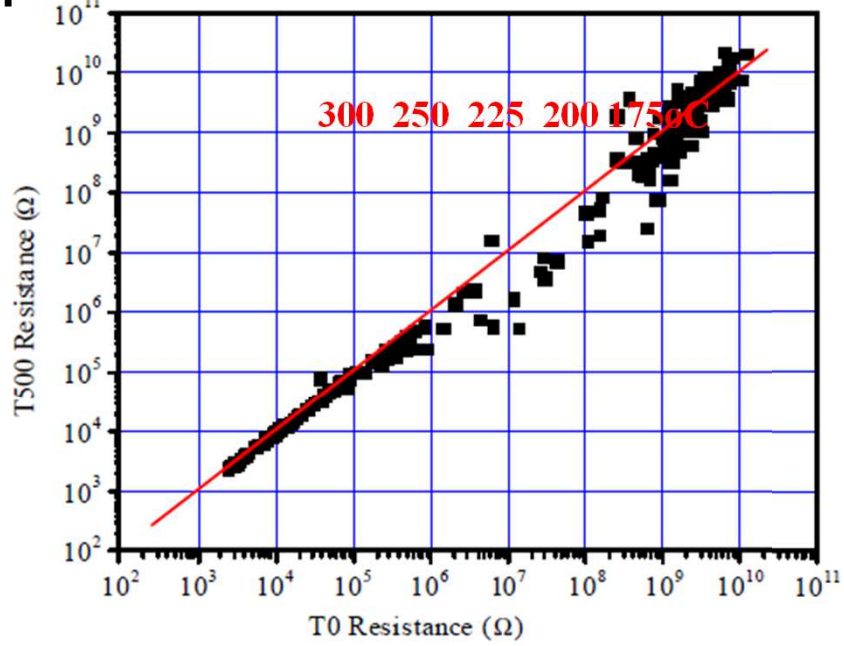


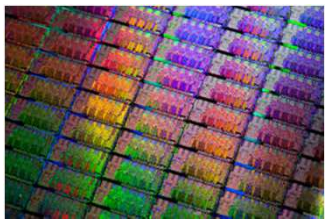
Figure 4. Very little resistance change observed in the fuses with resistance lower than 1MΩ after 500 hrs HTS at 150C, as well as after 500 cycles DTC stress.

RELIABILITY QUALIFICATION OF $CoSi_2$ ELECTRICAL FUSE FOR 90NM TECHNOLOGY

C. Tian, B. Park, C. Kothandaraman, J. Safran, D. Kim, N. Robson and SS. Iyer.

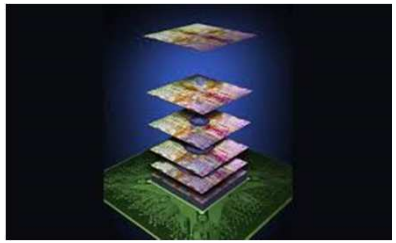
I-Fuse™: ZERO Defect

- **Field return is very costly**
  - 10x costs from wafer sort, packaged chip, module, PCB, to system
- **ZERO defect after shipping**
  - Defects should be found out and screened before shipping
- **I-fuse™ can achieve ZERO defect**
  - OTP dilemma: fully tested before shipping; but can't be used any more
  - Guarantee cell programmable: if initial fuse resistance <400Ω
  - Guarantee 100% programmable: if programmed within specs
  - Fully testable*: every functional block, including program circuits
    - Create non-destructive program state to read 1 for complex tests
    - Concurrent low-voltage PGM and read same cell => fake reading 1

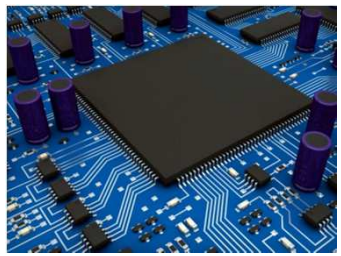


$0.1

$1



$10



$100

$1000

Conclusion: Non-Explosive I-Fuse™

- Low Program Voltage & Current
  - Small size
  - No charge pump
  - PGM voltage about core or I/O voltage
  - Short program time
- Deterministic programming behavior
  - Narrow resistance distribution
  - Easy to use (No HV device/circuit)
  - High reliability
  - High temperature
  - High data security
  - Fully testability
- Applications: AI, IoT, Automotive, Industrial, communication

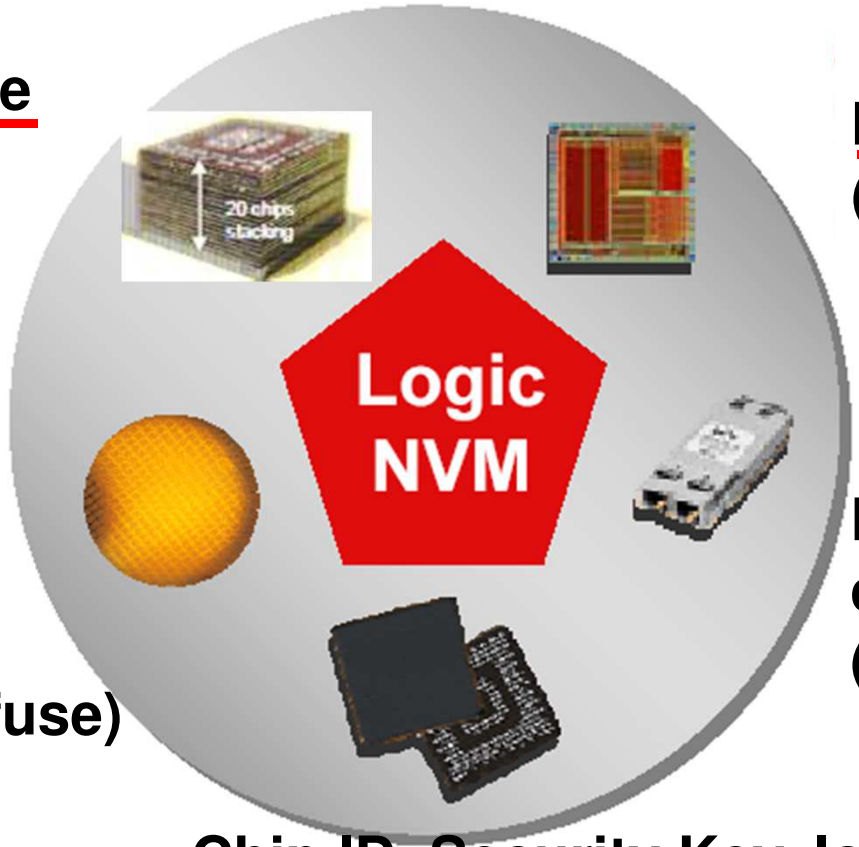
The only OTP programming mechanism can be modeled by physics: heat generation/dissipation and electro-migration

BACKUP

OTP Applications

- OTP (One-Time-Programmable): a memory IP be programmable only once to store permanent data
- OTP allows each IC to be customized after fabrication
  - Every chip needs OTP, if available, affordable, & reliable

Product feature selection



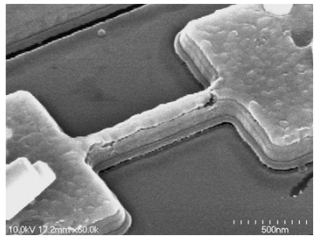
MCU code storage (replace flash)

3D IC repair Memory redundancy (replace laser fuse)

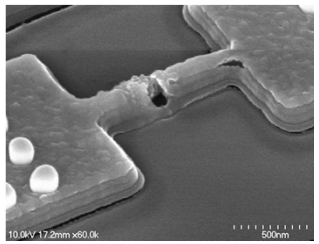
Device trimming / calibration (eliminate EEPROM)

Chip ID, Security Key, IoT

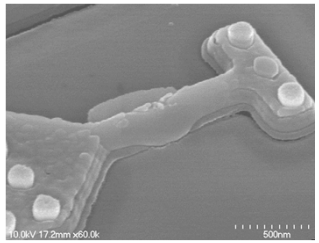
E-fuse



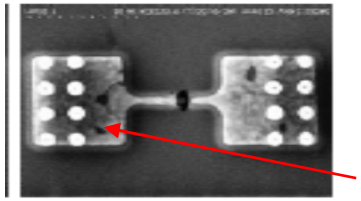
Electro-migration



Rupture



Melt

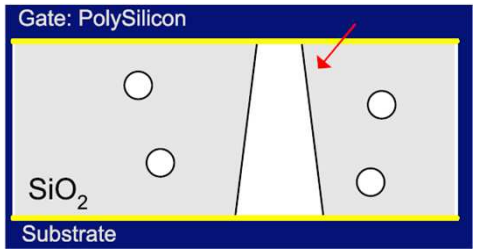


Debris

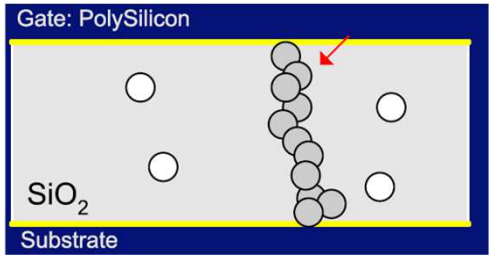
A Commercial Field-Programmable Dense
Array Memory with 99.999% Sense Yield f
SOI CMOS

Defect: 1E-5 (IBM)

Gate oxide Breakdown



Hard breakdown

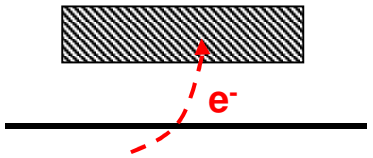


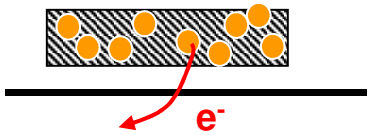
Soft breakdown

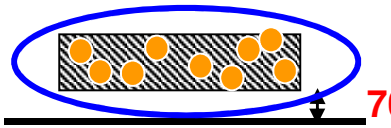
Ultra-Thin Gate Dielectrics:
They Break Down, But Do They Fail?
IEDM 97-73

We study breakdown in high-quality 2-7nm gate dielectrics, and find that soft breakdown becomes more likely for thinner oxides and for oxides stressed at lower voltages. For 2nm oxides, an increase in gate noise is the only precise indication of soft breakdown. For many applications, devices should remain functional with the level of gate noise we have observed, after soft breakdown.

Logic EPROM







70A: 0.35um MOS

- Only good for 0.35/0.5um CMOS
- Data retention

Efuse vs. I-Fuse™

- **Revolutionary I-fuse™ fixes all problems in eFuse**
  - **Reliability & qualification guaranteed by physics**
  - **Robust OTP technologies NOT to cause any problems**

28nm and beyond	eFuse*	I-fuse™
Program current	Up to 100mA	<3mA
HTS qual	4Kb passed 125°C 1Khr with 2 cells per bit	256Kb passed 250°C 1Khr without any redundancy
Read time in life	< 1sec	Unlimited read time
Program yield	A few % loss	~100%
Scalability	NO	YES
Testability	NO	YES. Achieve ZERO defect

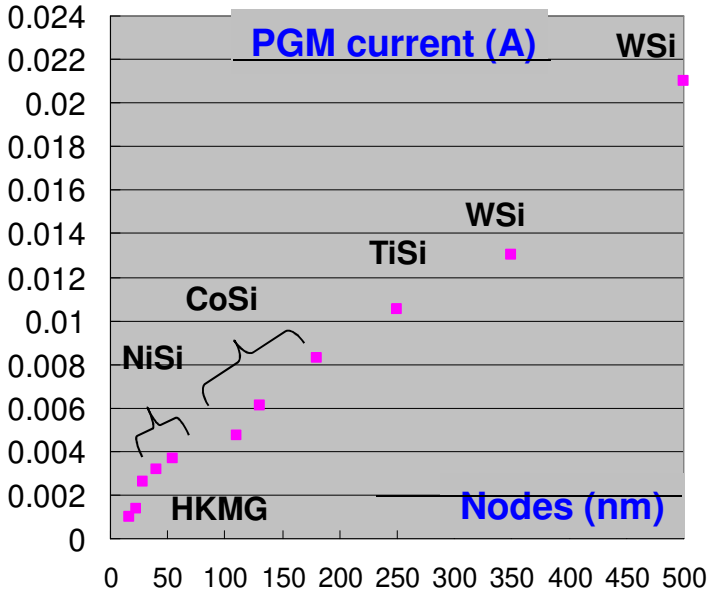
* Customers testimonies

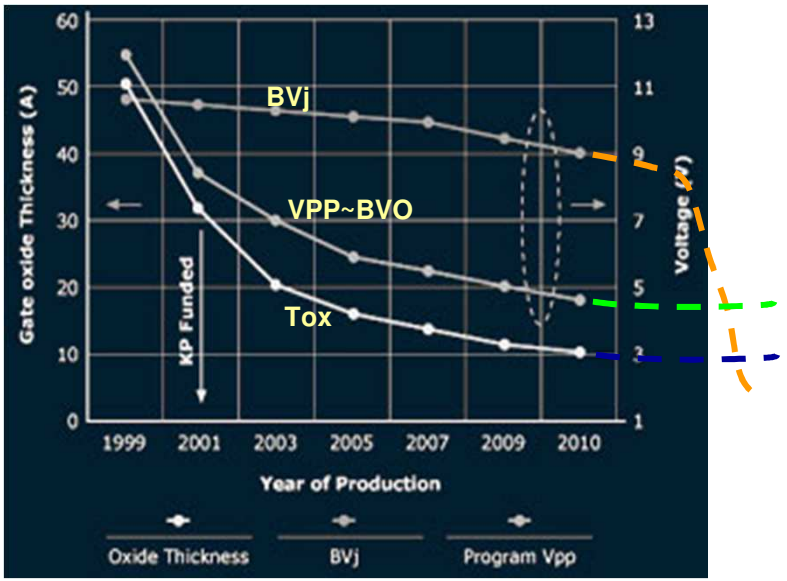
Beyond 28nm: I-Fuse™ vs. Anti-Fuse(AF)

- Narrower fuse => low PGM current
- Low PGM current => low PGM volt.
- I-fuse™ scalable to 14/7/5/3/2/1nm
- Non-breaking I-fuse wins breaking

- Supply voltages lower and lower
- Oxide/PGM voltage can't scaled
- Junction breakdown before oxide
- AF Hard to work beyond 14/16nm

Fuse current programming prevails AF voltage programming !!!
Non-explosive I-fuse™ prevails explosive eFuse !!!



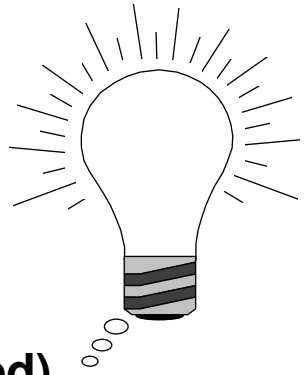


BVJ/BVO: Breakdown voltage of junction/oxide

I-fuse™: current PGM

Anti-fuse: voltage PGM

The Team



- Founder: Shine Chung
- Harvard graduate in Applied Physics
- 30 years of IC design experience
- Memory design in AMD, Intel, and HP
- PA-WW architect (PA-WW: precedent of Intel's Merced)
- Director at TSMC (eFuse pioneer)
- VLSI and ISSCC technical committee for 4 years
- Two-time TSMC innovation award recipient
- 61 patents granted before Attopsemi
- Filed >65 U.S. patents and 54 granted after Attopsemi

- Co-founder & VP of Eng: WK Fang
- MSEE from Ann Harbor, U. of Michigan
- 20-year experiences in memory
- Technical Manager at TSMC
- Department Mgr for eFuse
- Design managers for N90/N65 SRAM TV, eDRAM
- MTS in SRAM, FIFO, CAM at IDT

BACKUP