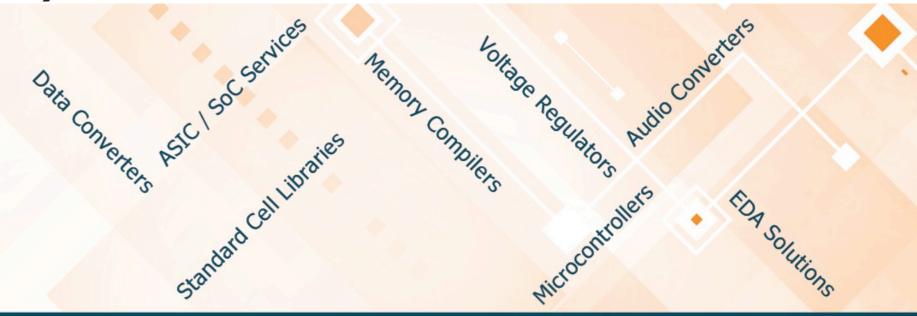


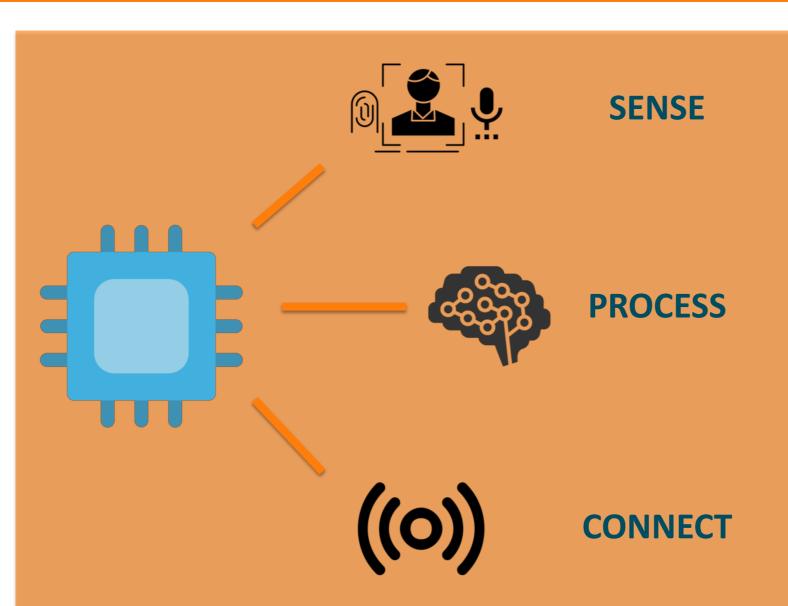
FD-SOI Adaptive Body Bias solutions to accelerate energy-efficient SoC designs

PIERRE GAZULL - BUSINESS DEVELOPMENT & PRODUCT MARKETING MANAGER

Chip
2019 TEL AVIV - MAY 13TH









Increase Battery Autonomy

Boost Performances





Reduce Time-to-Market



Active

SoC running - All blocks ON

μA / MHz

Active-Low Power, Sleep

SoC running in low-power mode

MCU OFF - RF OFF - Peripherals are active

 $\mu A / MHz$

Deep Sleep, Trigger,

Logic Domain & SRAM in retention mode IO and AON/RTC active

 $< 1 \mu A$

Stop

Logic domain OFF - SRAM OFF IO disabled - AON/RTC active

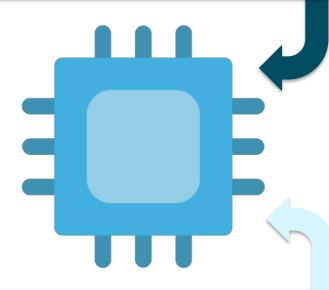
< 500 nA

Shut Off

Only wake-up pin remain active AON/RTC is OFF

< 200 nA

Energy-Efficient IP for Mostly-Off Domain



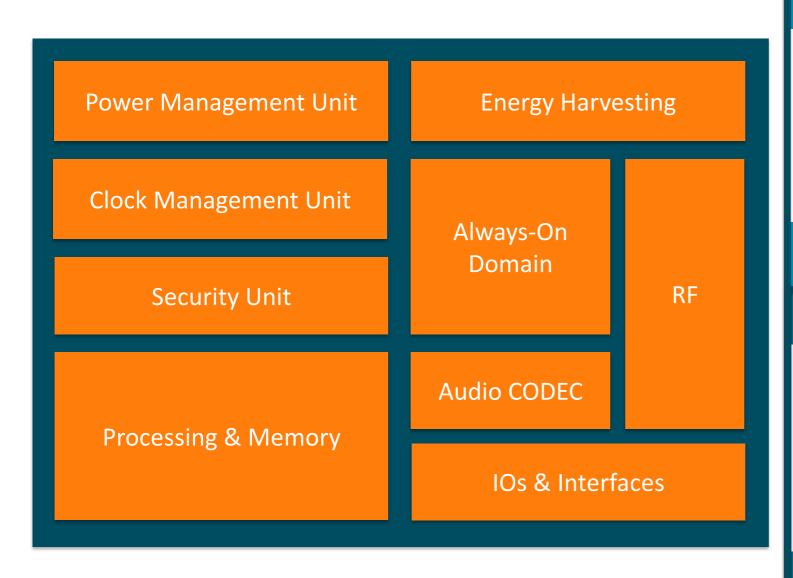
Low Leakage IP

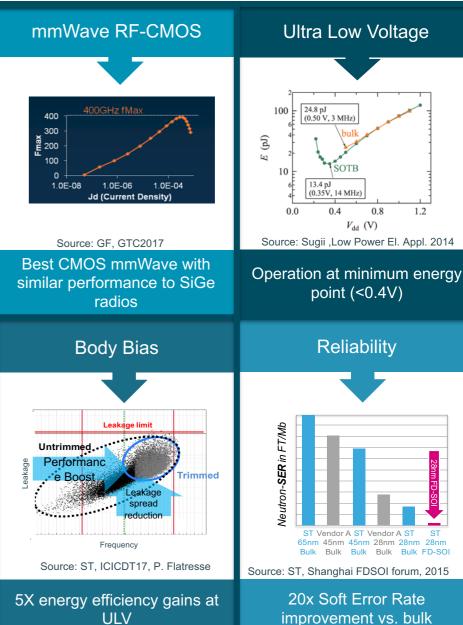
for Sleep Mode & AON Domain









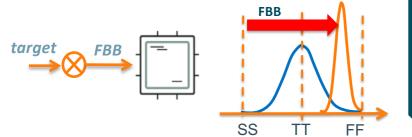


BODY-BIAS: A KNOB FOR ENERGY-EFFICIENCY





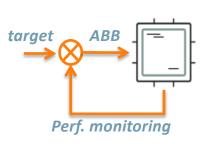
- Intrinsic radiation hardness
- Body-bias **boost** mode

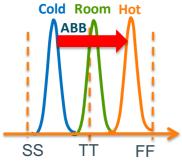


Now

Past

• Static FBB for process variations trimming





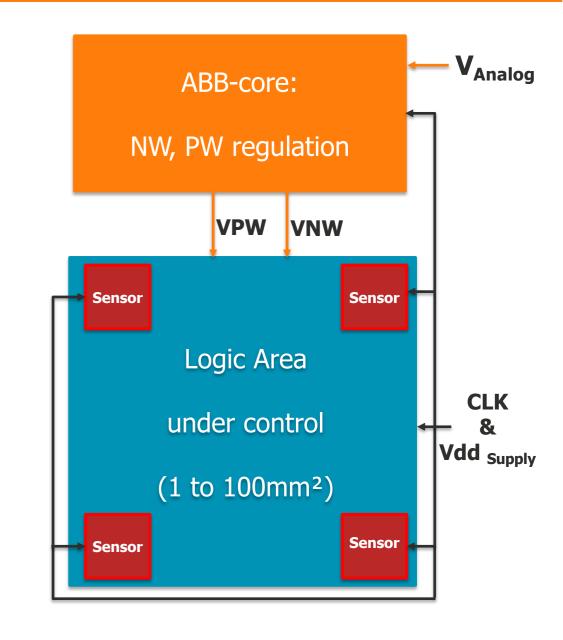
speed

Future

- Adaptive Body Bias (ABB) for compensating
 - Temperature variations in Low V_{dd} range
 - Aging variations in Nom to High V_{dd} range



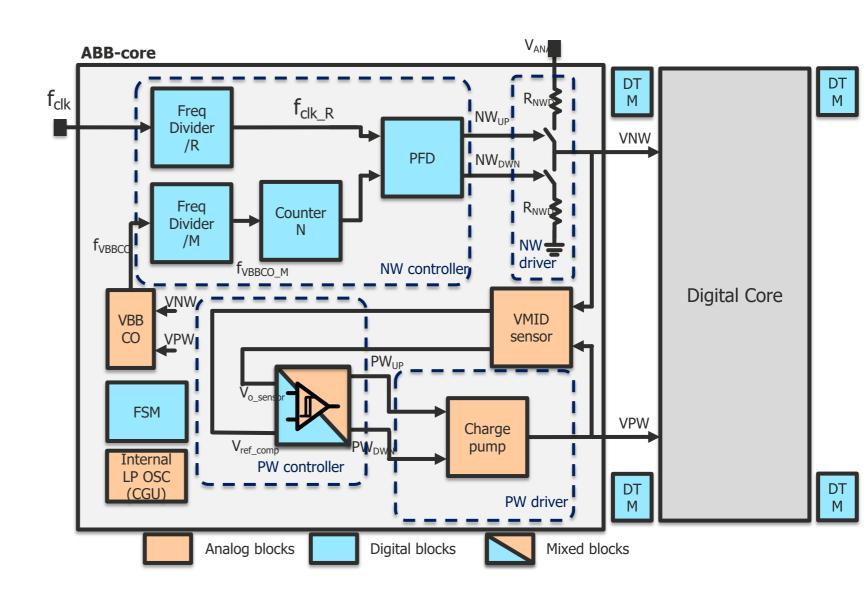
- ABB IP for Process, Voltage, Temperature & Aging compensation
- All-in-one IP including body-bias voltage regulator,
 low power sensors and control loop
- Foundation IP independent
- Ultra wide voltage range: 0.4V to 0.945V
- < 1% area overhead vs. logic area
- < 10 μW power overhead



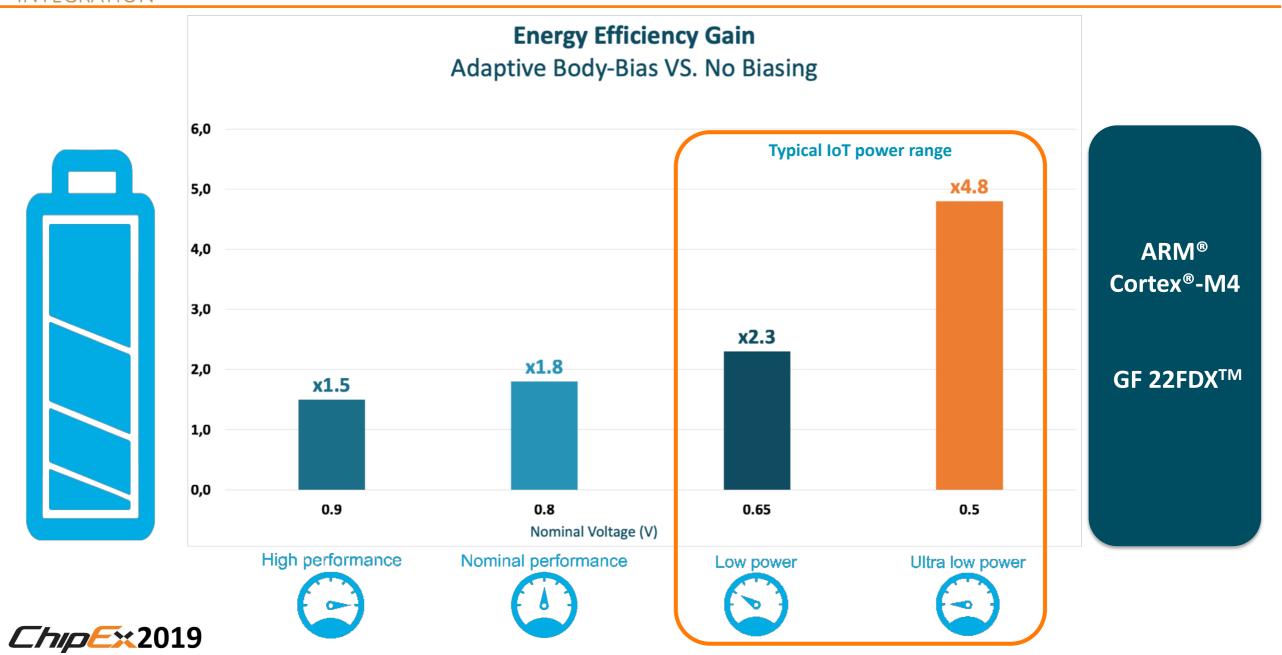


2 Sensors

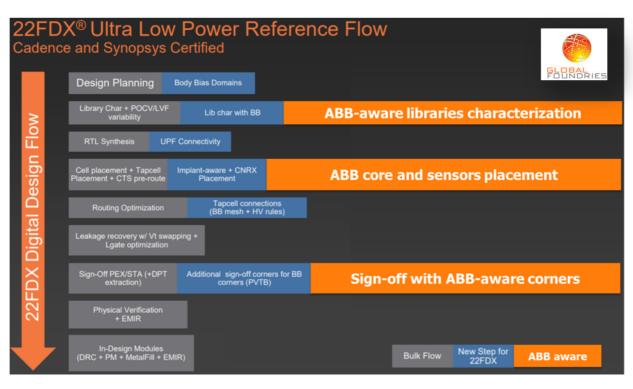
- → VBBCO monitor for coarse-grain compensation
- Distributed Timing Monitors
 (DTM) for fine-grain
 compensation
- 2 independent N- & P-WELL regulation loops
 - → VNW regulation refers to Fclk
 - → VPW regulation refers to VNW

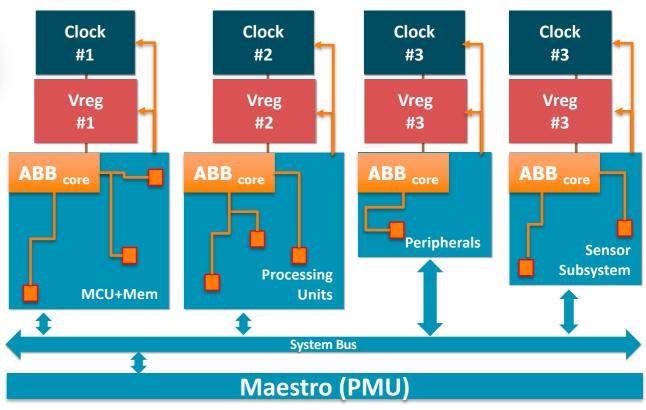


PPA IMPROVEMENT WITH ADAPTIVE BODY-BIAS



ADAPTIVE BODY-BIASING IN 22FDXTM SoC DESIGN FLOW





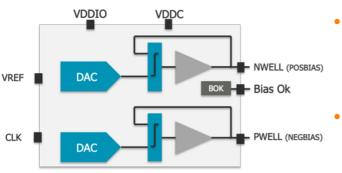
Seamless Integration in 22FDXTM Design Flow

Scalable to any SoC Architecture



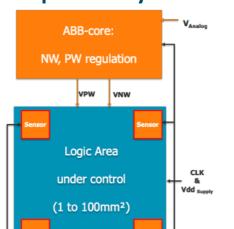
Page 9

Stand-Alone Body-Bias Generator



- **Several configurations** to support various loads size
- Ultra low current consumption < 10μW in active/shutdown mode

Adaptive Body-Bias for Mostly-Off Domain



- **All-in one IP** for PVTA compensation
- **Ultra Wide voltage range**
- < 1% area overhead vs. logic area

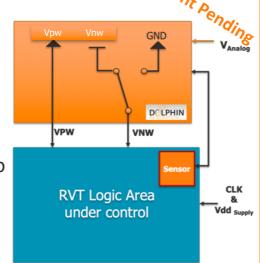
Energy-

Efficiency

< 10µW power overhead

Zero Power BBGEN for Always-ON Domain

- **AON** is dominated by leakage
- Hungry charge pump not an option
- **RBB** only as an attractive solution to reduce leakage



Energy-Efficiency is a function of PVT sensors accuracy

Accuracy



SlackGuardTM: Aging monitors

Timing margin detection of critical paths

DTM: Delay Timing Monitor

Fine grain compensation

VBBCO: Body Bias Controlled Oscillator

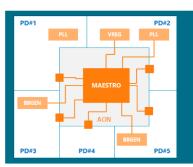
Coarse grain compensation



Scalable and configurable



POWER MANAGEMENT IP PLATFORM

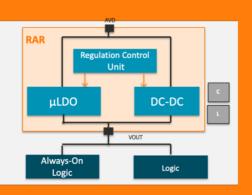


Embedded PMU/ACU

Boot-up sequence management

Body-Bias, DVFS, AVS support

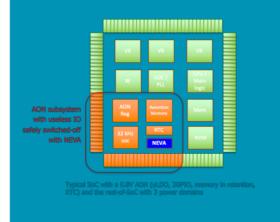
Voltage Regulators



High Efficiency DC/DC Ultra-low quiescent LDO

95% Efficiency Quiescent down to 150 nA

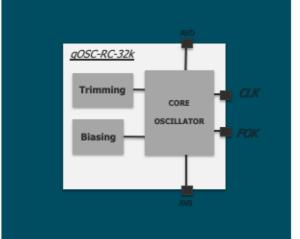
Power Gating Solutions



Ultra-low leakage IO & logic power gating

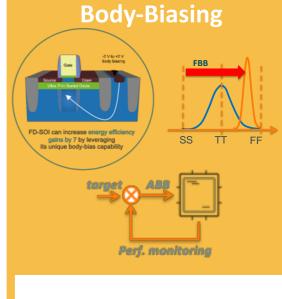
IO Leakage reduction up to x14

uLP Oscillators



32 kHz RC & XTAL

Ultra Low power < 80 nA



PVTA Compensation

5x Energy-Efficiency ABB 7x Energy-Efficiency ABB + AVS



