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Shaping the future of the connected world with FinFET and FDSOI

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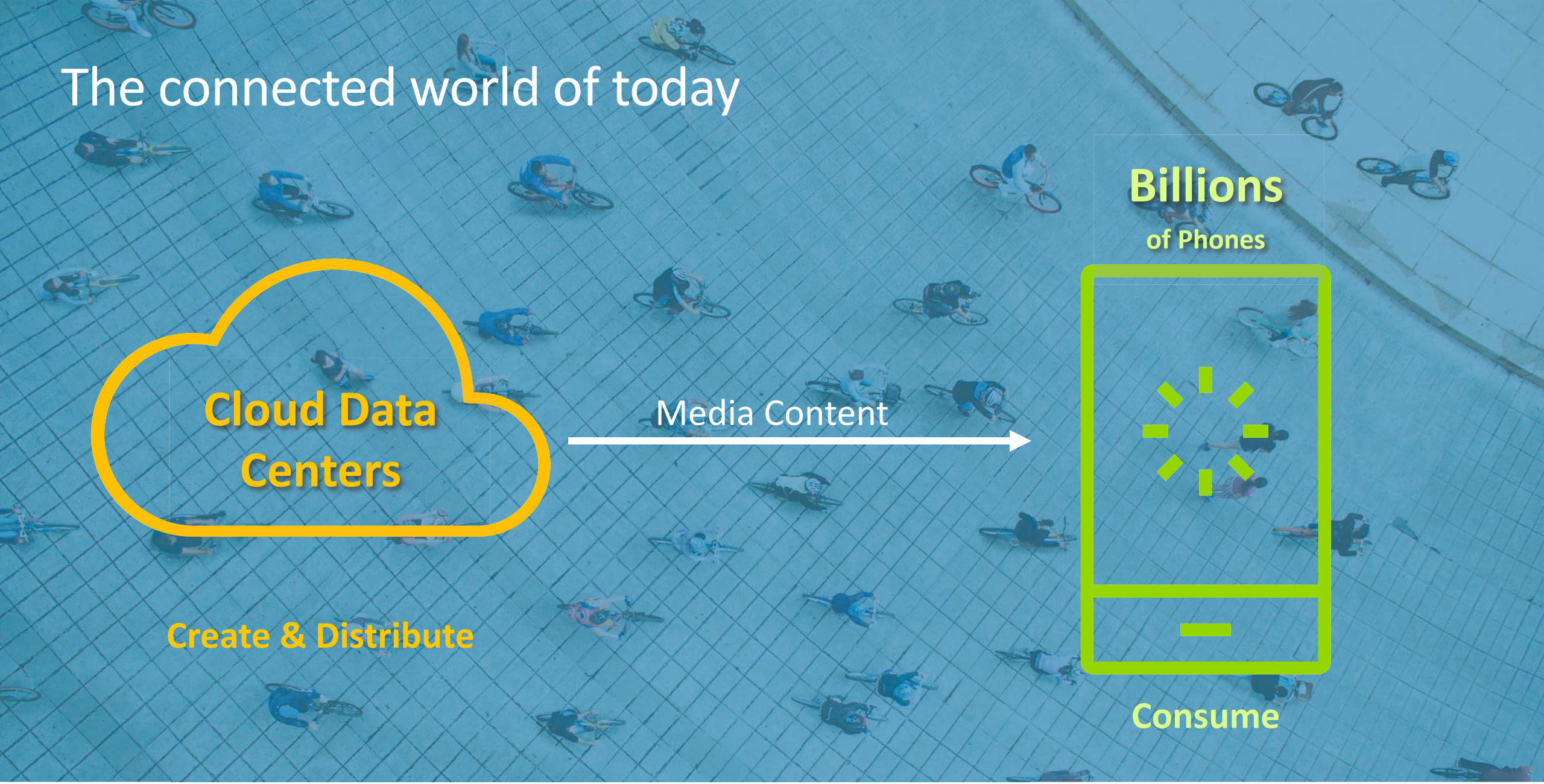
13th May 2019

The connected world of today



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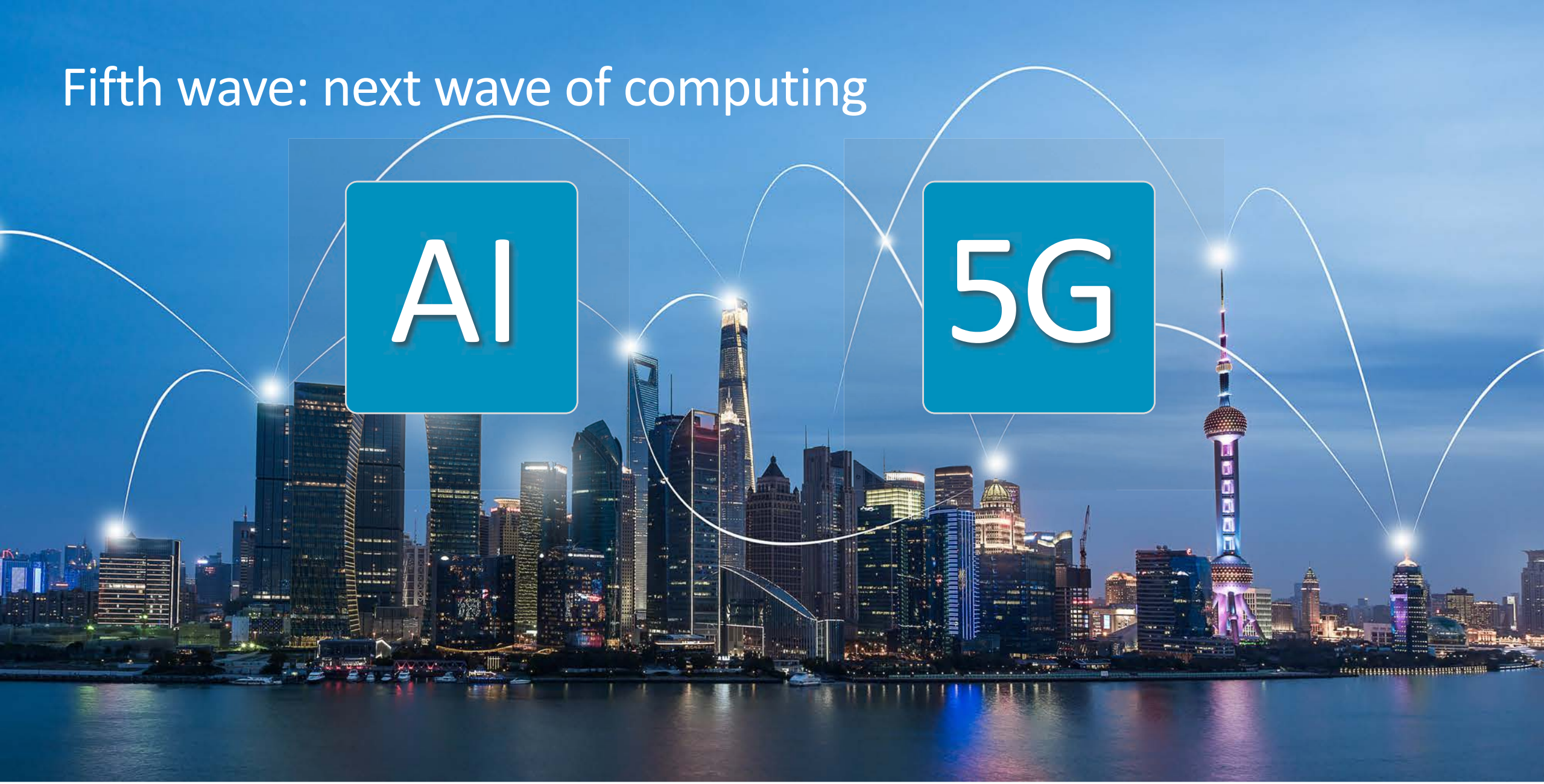
Fifth wave: next wave of computing



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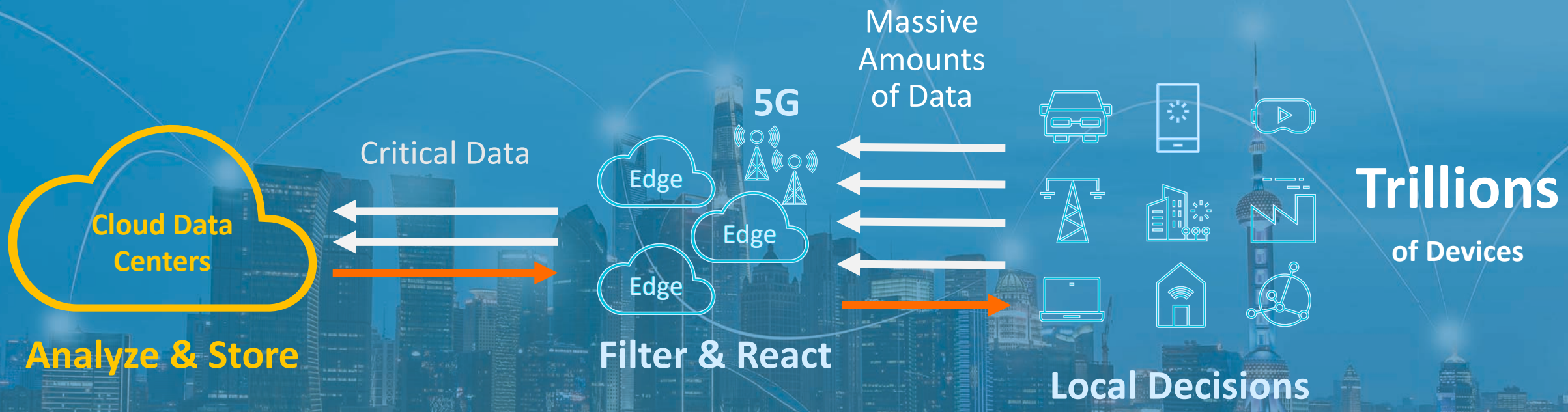
Looking ahead to a new connected world



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But different markets have different needs

Mobile and Consumer

- High performance
- Low power
- Cost (area) sensitive
- Flexible performance requirements

Mainstream
- 16/14/12/11nm
- 10/8nm

Premium
- 7/5nm

Networking and Servers

- High performance
- Fault tolerance
- Long lifetime
- Continuous operation

Networking
- 7/5nm
- 16/14/11nm
- 10/8nm

Server
- 7/5nm

Automotive

- High temperature
- Fault tolerance
- Long lifetime
- Low power
- Non-volatile memory

Engine & Body Control
- 55/40nm
- >130nm

ADAS, self driving
- 7nm
- 16/14nm
- FDSOI
- eMRAM

IoT

- Very low power
- Low voltage
- Very low cost
- Non-volatile memory

Ultra Low Power
- >40nm
- 28/22nm
- eMRAM
- FDSOI

Advanced Applications
- 16/14/12/11nm

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Foundry market snapshot

Foundry Market by Feature Dimension

	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027
≤5nm ($M)	**--**	**--**	**--**	**374**	**3,785**	**6,495**	**8,794**	**10,961**	**13,264**	**15,896**	**18,958**
Growth rate (%)	--	--	--	NA	912.03	71.60	35.40	24.64	21.01	19.84	19.26
7nm ($M)	**--**	**3,071**	**11,194**	**12,931**	**13,253**	**13,337**	**13,412**	**13,475**	**13,486**	**13,456**	**13,423**
Growth rate (%)	--	NA	264.51	15.52	2.49	0.63	0.56	0.47	0.08	(0.22)	(0.25)
10nm ($M)	**4,692**	**4,770**	**2,581**	**2,490**	**2,362**	**2,152**	**1,927**	**1,637**	**1,340**	**1,151**	**989**
Growth rate (%)	NA	1.66	(45.89)	(3.53)	(5.14)	(8.89)	(10.46)	(15.05)	(18.14)	(14.10)	(14.07)
16/14/12nm ($M)	**10,857**	**11,453**	**10,138**	**9,091**	**8,611**	**7,914**	**7,540**	**7,270**	**6,948**	**6,651**	**6,447**
Growth rate (%)	NA	5.49	(11.48)	(10.33)	(5.28)	(8.09)	(4.73)	(3.58)	(4.43)	(4.27)	(3.07)
28/22/20/18nm ($M)	**11,802**	**9,782**	**8,862**	**8,617**	**9,022**	**9,759**	**10,623**	**11,596**	**12,735**	**13,956**	**15,216**
Growth rate (%)	NA	(17.12)	(9.41)	(2.76)	4.70	8.17	8.85	9.16	9.82	9.59	9.03
45/40nm ($M)	**7,825**	**7,287**	**6,725**	**6,545**	**6,741**	**6,816**	**6,737**	**6,668**	**6,584**	**6,496**	**6,401**
Growth rate (%)	NA	(6.88)	(7.71)	(2.68)	2.99	1.11	(1.16)	(1.02)	(1.26)	(1.34)	(1.46)
65nm ($M)	**7,153**	**6,742**	**6,416**	**6,326**	**6,515**	**6,529**	**6,518**	**6,503**	**6,484**	**6,462**	**6,432**
Growth rate (%)	NA	(5.75)	(4.84)	(1.40)	2.99	0.21	(0.17)	(0.23)	(0.29)	(0.34)	(0.46)
90nm ($M)	**1,982**	**1,836**	**1,863**	**1,795**	**1,771**	**1,733**	**1,681**	**1,628**	**1,573**	**1,516**	**1,459**
Growth rate (%)	NA	(7.37)	1.47	(3.65)	(1.34)	(2.15)	(3.00)	(3.15)	(3.38)	(3.62)	(3.76)
0.13µm ($M)	**4,502**	**4,591**	**4,225**	**4,038**	**4,142**	**4,295**	**4,418**	**4,530**	**4,642**	**4,740**	**4,830**
Growth rate (%)	NA	1.98	(7.97)	(4.43)	2.58	3.69	2.86	2.54	2.47	2.11	1.90
0.18/0.15µm ($M)	**6,034**	**6,325**	**6,390**	**6,582**	**6,762**	**6,901**	**7,207**	**7,598**	**8,024**	**8,477**	**8,907**
Growth rate (%)	NA	4.82	1.03	3.00	2.73	2.06	4.43	5.43	5.61	5.65	5.07
≥0.25µm ($M)	**5,022**	**5,298**	**5,563**	**5,784**	**6,017**	**6,315**	**6,676**	**7,093**	**7,601**	**8,181**	**8,813**
Growth rate (%)	NA	5.50	5.00	3.97	4.03	4.95	5.72	6.25	7.16	7.63	7.73
TOTAL ($M)	**59,869**	**61,155**	**63,957**	**64,573**	**68,981**	**72,246**	**75,533**	**78,959**	**82,681**	**86,982**	**91,875**
Growth rate (%)	NA	2.15	4.58	0.96	6.83	4.73	4.55	4.54	4.71	5.20	5.63

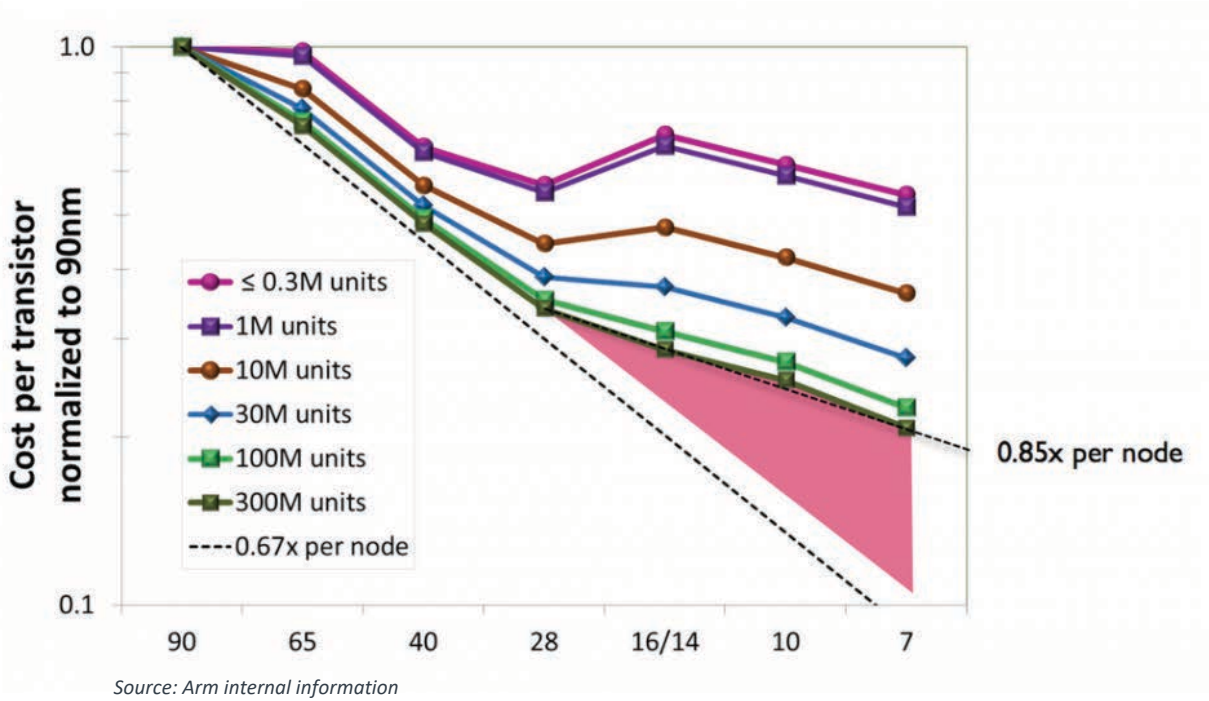
Source : IBS data 2018

Summary

- 5nm & below expected to have double digit % growth largely driven by mobile and server requirements
- 7nm shows negligible growth
- 28/22/18nm shows strong growth

But advanced designs are not for everyone

Gate cost trends



Source: Arm internal information

- There is still a cost benefit to move to advanced nodes if your volume is high for digital logic dominated SoC's
- Around 10M units, the benefit of moving to advanced nodes diminishes, even for digital logic
- Analog IP does not shrink in the same way, so staying around 28nm becomes a good node

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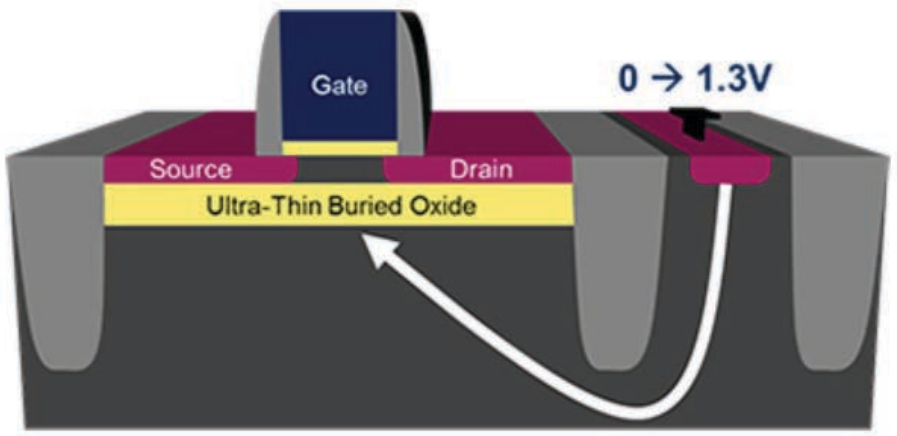
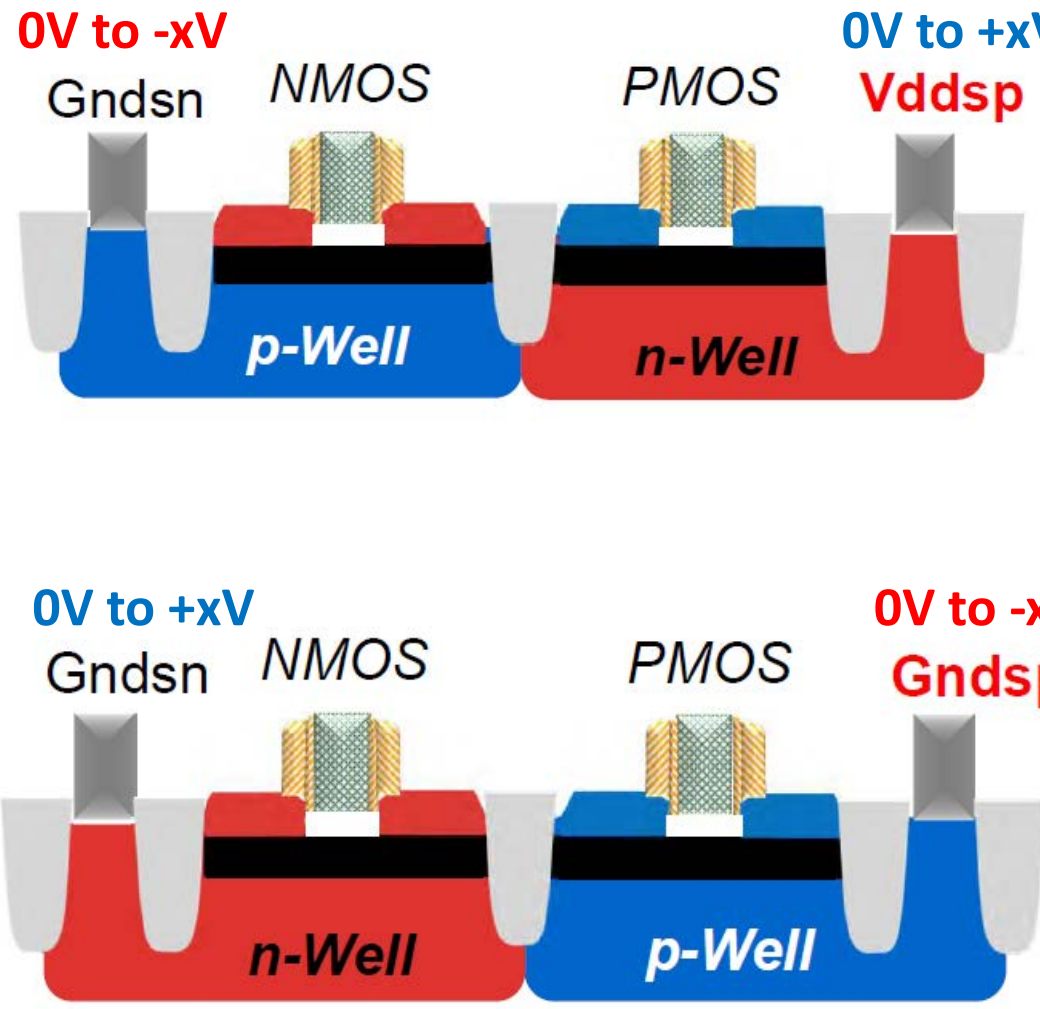
Step into the world of FDSOI

Key differentiator with respect to FinFET & Bulk

Speed/Power optimization



- Modulate transistor Vt for speed / power control
- No area penalty compared to bulk



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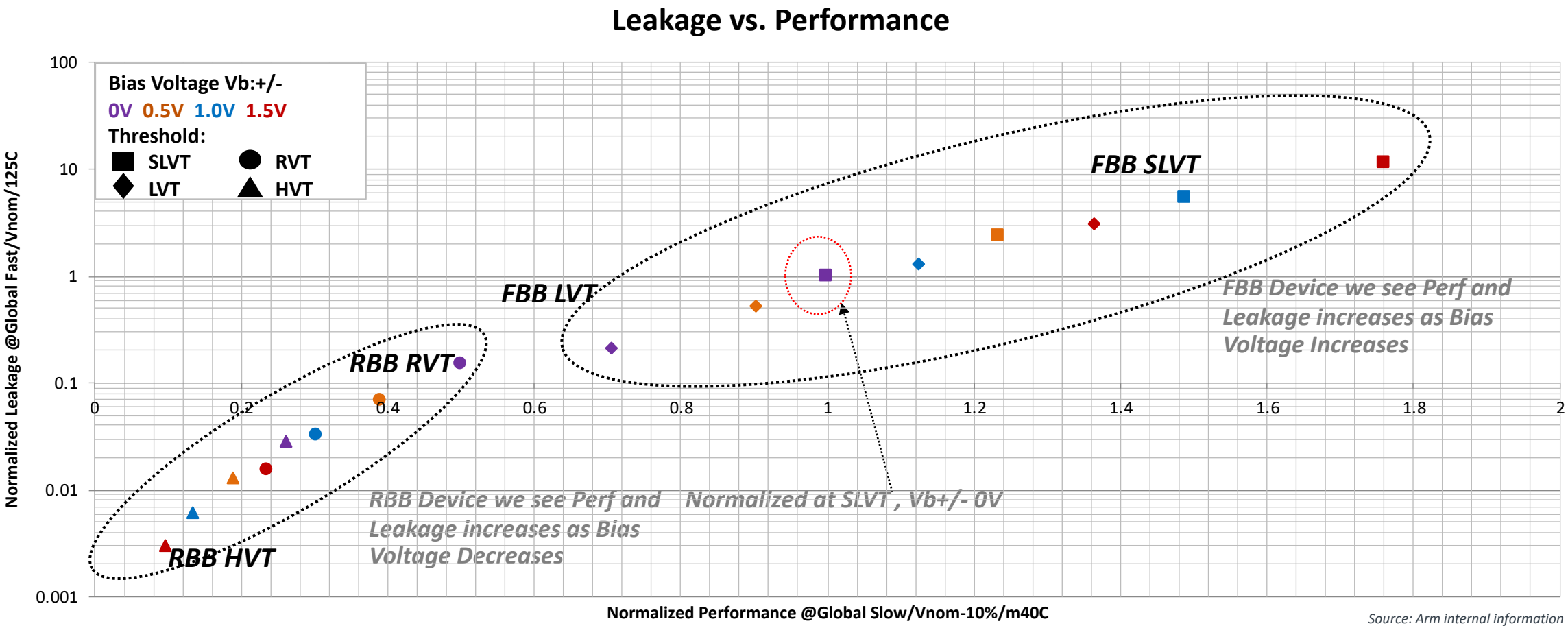
Wide-range of design optimization points



Source: Arm internal information

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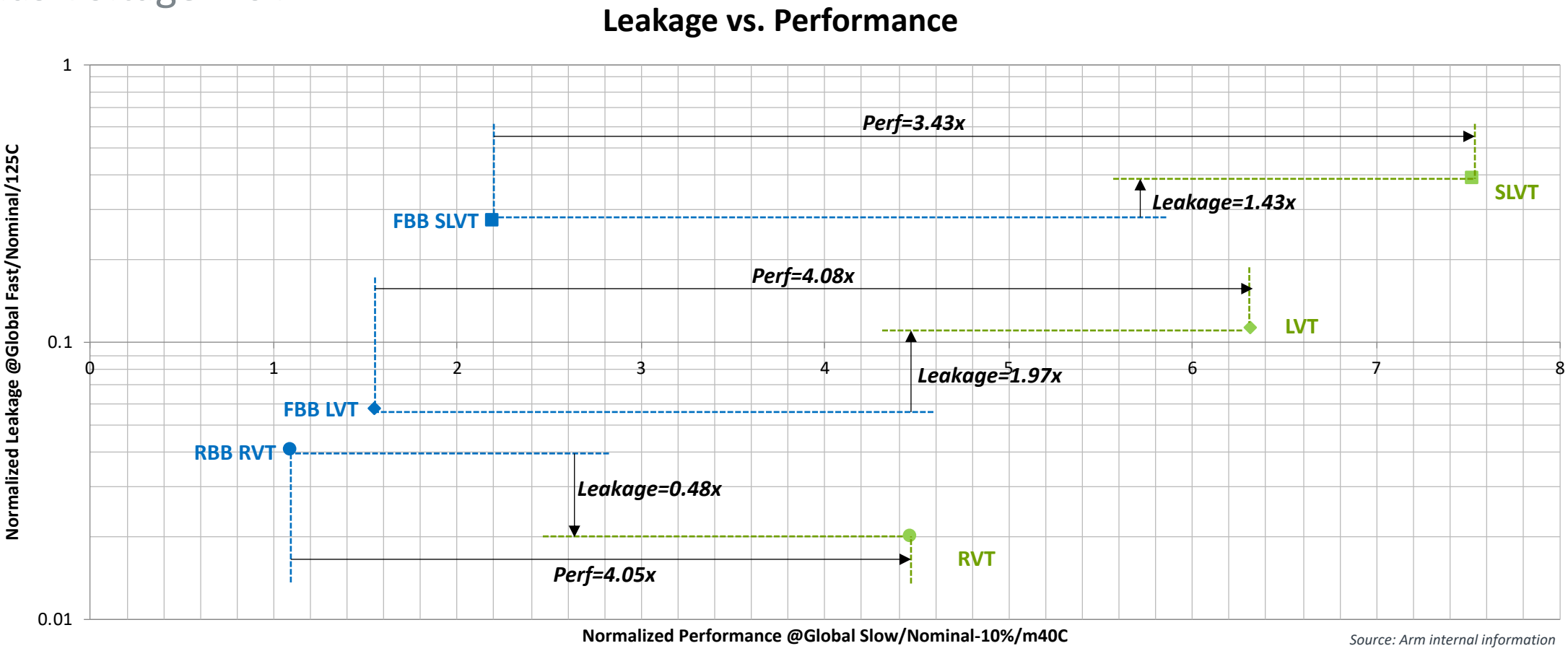
A comparison between FDSOI and FinFET @Global Corner

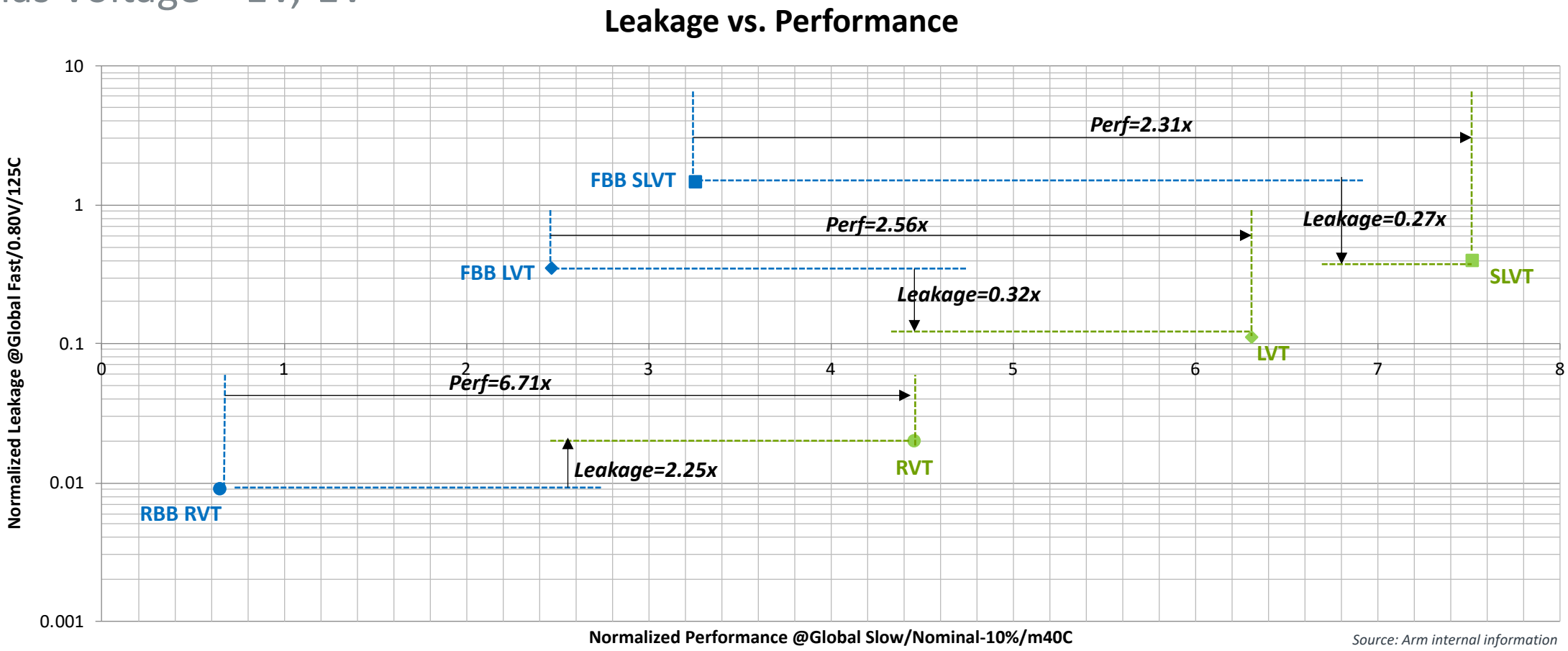
Bias Voltage = 0V



Source: Arm internal information

A comparison between FDSOI and FinFET @Global Corner

Bias Voltage = 1V,-1V



Source: Arm internal information

DVFS vs Body Bias

Need lot of PVT corners to take advantage of body bias

PVT List for DVFS

Domain	Process	Logic VDD (V)	Core VDD (V)	Temp ('C)
NOM (0.8v)	SSPG	0.72	0.72	-40
	SSPG	0.72	0.72	125
	SSPG	0.72	0.72	0
	FFPG	0.88	0.88	-40
	FFPG	0.88	0.88	125
	FFPG	0.88	0.88	0
	TT	0.8	0.8	0
	TT	0.8	0.8	25
	TT	0.8	0.8	85c

PVT List for Body Bias

Domain	Process	Logic VDD (V)	Core VDD (V)	Nwell body-bias (V)	Pwell body-bias (V)	Temp ('C)
NOM (0.8v)	SSPG	0.72	0.72	0.4	0.4	-40
	SSPG	0.72	0.72	0.4	0.4	125
	SSPG	0.72	0.72	0.8	0	0
	FFPG	0.88	0.88	1.4	-0.6	-40
	FFPG	0.88	0.88	1.4	-0.6	125
	FFPG	0.88	0.88	0.8	0	0
	TT	0.8	0.8	0.8	0	0
	TT	0.8	0.8	0.8	0	25
	TT	0.8	0.8	0.8	0	85c
	TT	0.8	0.8	1.1	-0.3	25
	TT	0.8	0.8	1.4	-0.6	25
	TT	0.8	0.8	0.4	0.4	25

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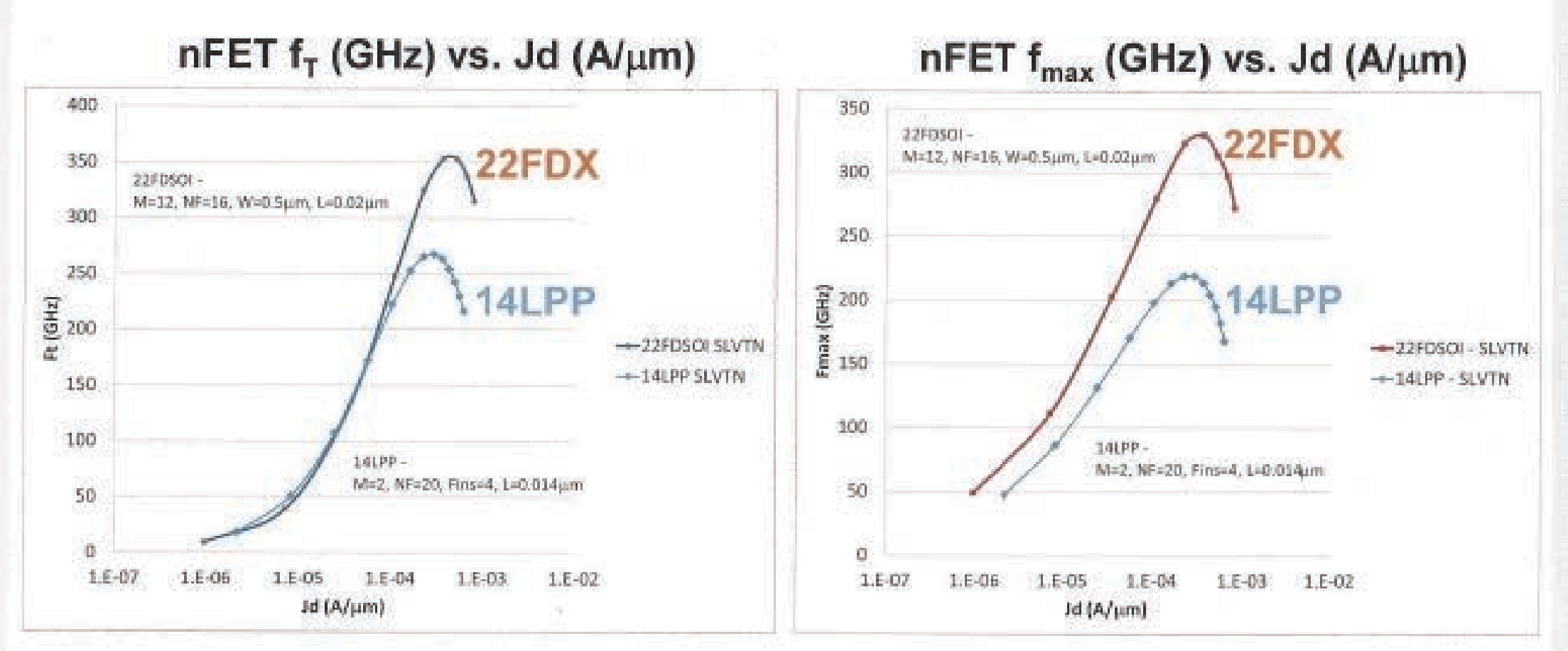
Moving to Radio Frequency (RF)

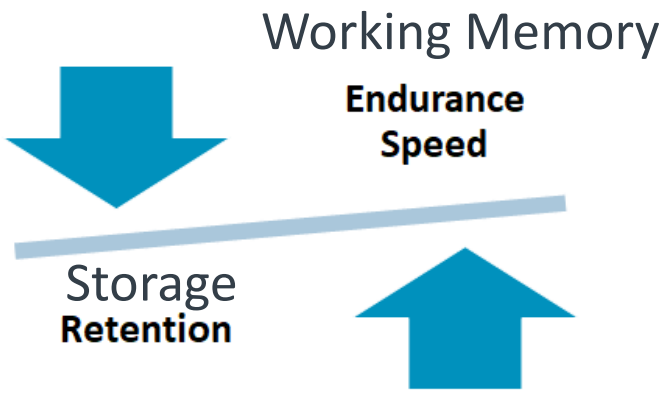


FDSOI shows better f_T and f_{max} than FinFET

eMRAM: Non-volatile Memory Solution for FDSOI

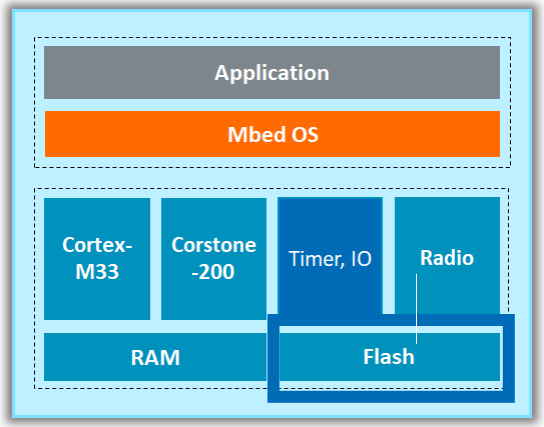
Embedded storage and working memory applications

Application-specific tuning



eMRAM for storage

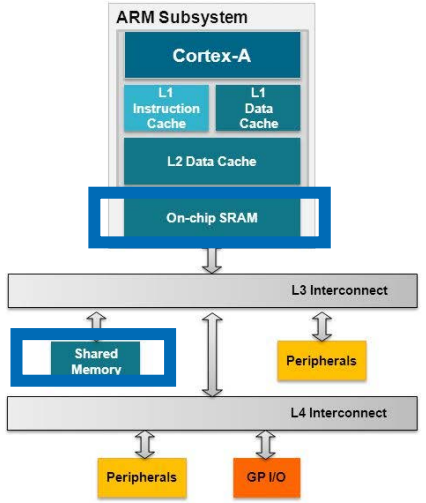
Working memory for SoC providing area, power and BoM savings



Storage memory for MCU as eFlash becomes cost-prohibitive

eMRAM as working memory

Physics results in Retention vs. Endurance/Speed trade-off



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In closing

- FDSOI as a technology gives you the opportunity to reduce the bill of materials due to availability of Non-volatile memories, RF, compute horse power through biasing and knobs for power management.
  - To allow a higher adoption for FDSOI will need
    - A larger ecosystem
    - EDA tooling support
    - IP vendors who can provide guidance to navigate and use the right knobs for your design points

- FinFET is a well established process and people will continue to use this to push for compute performance and density where volume matters
  - Design complexities are being lessened due to introduction of EUV, leading to better yield
  - Cost is an inhibitor and it lacks the richness of the FDSOI process when it comes to IoT kind of applications

Silicon is the way to a connected world

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Thank You
Danke
Merci
谢谢
ありがとう
Gracias
Kiitos
감사합니다
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شكرًا
תודה