Empirical ESD Simulation

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Introduction

- Simulation of electrostatic discharge (ESD) protection circuits may prevent ESD failures and shorten IC’s time to market, and save IC area due to ‘over-protection’
  - The simulation may ensure that the current through interconnects or protection devices does not exceed damaging value
  - Voltage drop along the ESD path does not exceed core breakdown
- The verification of ESD protection in a complex integrated circuit design is extremely challenging since the ESD devices are commonly based on snapback
  - Compact models are very complex and difficult to develop
  - The I-V characteristics are not 1-1 curves
ESD Window and Limitations

- **ESD device limitation:** Thermal breakdown at $V_{t2}$, $i_{t2}$
- **Dynamic voltage clamping:** The core devices (to be protected) should not be exposed to voltage above their breakdown at any time
- **Current density limitation of interconnects**
Voltage Clamping Example

‘Open drain’ Input ESD protection:
Positive zap between Vdd pin and Input pin
ESD path through ESD rails, power-clamp (snapback), ESD transistor (diode)

\[ V_{gs,M2} = I_{ESD} \times (R_{bus,2} + R_{bus,3} + R_{bus,4}) + V_{on,DT2} + I_{ESD} \times R_{on,DT2} + V_{h,PC} + I_{ESD} \times R_{on,PC} < V_{BD} \]
Dynamic Triggering of ESD paths

‘CMOS’ Input ESD protection: Positive zap between Input pin and Vss.

Different ESD paths may trigger, at different times, during the ESD event. ESD current conductance may be shared by two branches.

→ Dynamic simulation is required
• I(t) in circuit nets
• V(t) at circuit nodes
Empirical ESD Model Concept

The ESD transistor model is composed of the transistor pcell, with regular SPICE model, and a parallel ‘bipolar’ model generated by VerilogA code. The bipolar triggering is based on the voltages simulated on the ESD transistor terminals, during the discharge.

- As long as $V_{DS}(t)<V_{t1}(V_{GS}(t))$, regular device SPICE model is employed (MOSFET off). When $V_{DS}(t)$ reaches $V_{t1}$, a function representing TLP I-V curve after snapback, is added.

$V_{t1}$ results from TLP measurements of ESD transistors, at various $V_{gs}$.
ESD Transistor ‘sub-circuit’ Empirical Model

(1) ESD transistor pcell.
(2) Symbol representing bipolar VerilogA code
(3) Self bulk-drain diode.
(4) VerilogA code sub-circuit for diode Ron, based on TLP (when the self-diode is forward biased)
(5) Added circuit (ggnmos as an example)
(6) ESD stress source (current ramp, HBM/MM waveform)
ESD Simulation Flow

Simulation
- Identify ESD devices in scheme/layout

Scheme
- Add estimated resistors representing segments of ESD paths

Layout
- Extract parasitic resistances/capacitances

Apply ESD waveform

Simulation

Flag breakdowns

Breakdown data:
- ESD devices $i_{t2}/v_{t2}$
- $V_{BD}$ of non-ESD devices (at various terminals biases)
- Interconnects current density
Test Case 1, Gate Grounded Transistor – 2kV HBM

- Simulation of 5V NMOS ESD transistor, gate-source short
  - Max/min $V_{IO}$ is consistent with measured $V_{t1}(V_{gs}=0)$ and $V_{h}$
  - Simulations with various $V_{gs}$, were consistent with $V_{t1}(V_{gs})$ TLP measurements

- The spike of the current through the transistor $I(t)$, may be due to self discharge of the drain capacitance at bipolar turn on
Test Case 2, ESD NMOS with Soft Pull Down—2kV HBM

- 5V NMOS ESD transistor with soft pull-down. Positive HBM applied between drain to source.
- ESD transistor gate is floating and pulled up during the ESD due to capacitive coupling of the drain voltage rise. \( V_{t1} \approx 7V \) is consistent with ESD transistor \( V_{gs} \) rise to \( \approx 1.5V \).

\[ \begin{align*}
V_{t1} & \approx 7.5V \\
V_{h} & \approx 6V \\
V_{\text{drain}(t)} & \\
I(t) & \\
V_{\text{gate}(t)} & \\
I_{\text{leakage}}(A) & \\
I_{\text{DUT}}(A) &
\end{align*} \]
Test Case 3 – ‘CMOS’ I/O Protection

‘CMOS’ ESD protection scheme; ESD NMOS with soft pull-down, ESD PMOS with soft pull-up, GCNMOS power-clamp
Test Case 3 with Modeling Sub-Circuits
CMOS IO Protection – 4kV HBM I/O to Vss, Rbus=0

VerilogA massages during simulation: ESD devices identification and ESD events

IN - Width=360um, Ron=0.80ohm
IP - Width=360um, Ron=1.91ohm
IPC - Width=480um, Ron=1.01ohm
IN - Snapback on, Vgs=1.39V => Vt1=7.23V, Vh=6.20V, at 0.356ns
IPC - Snapback on, Vgs=3.71V => Vt1=6.48V, Vh=6.20V, at 1.488ns
IPC - Snapback off at 116.863ns
IN - Snapback off at 783.234ns
CMOS IO Protection - 400V MM I/O to Vss, Rbus=0

Poor voltage clamping!
Conclusions

- An empirical simulation for ESD protection circuits, containing snapback-based devices, has been demonstrated.
- The models of the ESD transistors combine regular SPICE model with TLP based curves, using VerilogA code. The ‘bipolar devices’ are triggered or turned-off, based on simulated $V_{gs}(t)$, $V_{ds}(t)$, and measured TLP $V_{t1}(V_{gs})$ and additional TLP curve key-points.
- The simulations are consistent with measured TLP curves.
- The simulations demonstrated the ability to check voltage clamping along ESD path, as well as ESD currents through the ESD devices and circuit nets.
- This methodology can be extended to all ESD devices used in various applications and voltage regimes.